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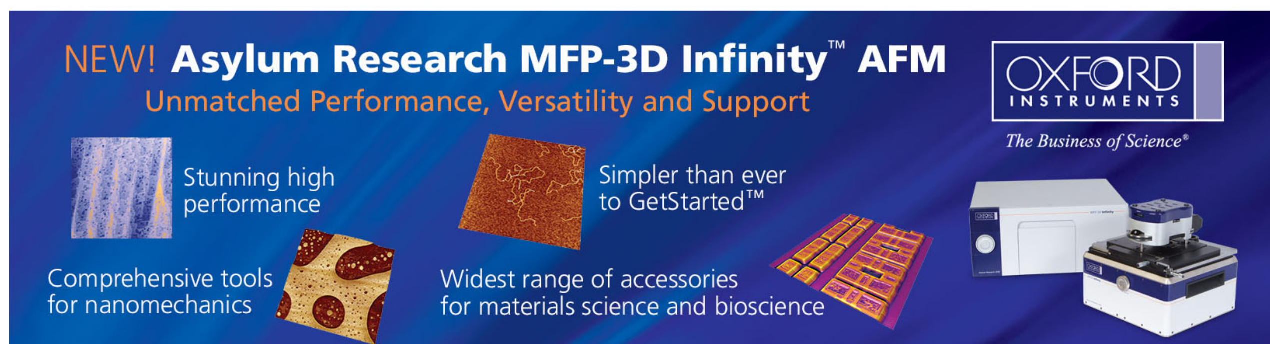

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Anomalous on-current and subthreshold swing improvement in low-temperature polycrystalline-silicon thin-film transistors under Gate bias stress

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This work investigates an improvement in anomalous on-current and subthreshold swing (SS) in Low-temperature polycrystalline-silicon thin-film transistors after positive gate bias stress. The experimental results reveal that the improved electric properties are due to the hole trapping at SiO_2 above the lightly doped drain regions, which causes a strong electric field at the gate corners. The effect of the hole trapping is to reduce the effective channel length and the SS. Besides, the stress-related electric field was also simulated by TCAD software to verify the mechanism above. © *2011 American Institute of Physics*. [doi:10.1063/1.3568895]

Low-temperature polycrystalline-silicon thin-film transistors (LTPS TFTs) have been widely investigated for flat-panel applications, such as for active matrix liquid crystal displays and active-matrix organic light-emitting diodes.[1,2] Compared to amorphous silicon TFTs (a-Si TFTs), LTPS TFTs have a higher electron mobility and driving current. Since the maximum process temperature is lower than 600 °C, LPTS TFTs can be fabricated on relatively cheap glass. Consequently, LTPS TFTs can integrate both the pixel array and peripheral circuits on the same glass substrate to realize a system-on-panel display.[3,4] It is well known, however, that device characteristics such as mobility, threshold voltage and subthreshold swing (SS) are usually degraded in LTPS TFTs due to the electrical stress.[5] Most previous studies have discussed the degradation mechanism in LTPS TFTs caused by the DC bias and dynamic stresses.[6,7] However, electrical stress induced improvement in device characteristics of n-channel LTPS TFTs has not been investigated carefully, and the mechanism has not been clearly identified. The purpose of this work is to investigate the improvement in on-current (I_{on}) and SS in LTPS TFTs after positive gate bias stress. The experimental result indicates that the improved I_{on} and SS originate from the hole trapping at the SiO_2 above the lightly doped drain (LDD) regions, which is caused by the strong electric field at the gate corner. In addition, the stress-related electric field was simulated by TCAD to verify the stress mechanism.

In this work, top-gate commercial n-channel LTPS TFTs with a LDD were prepared. First, a 500 nm thick buffer oxide was deposited on the glass. Next, 50 nm thick, undoped amorphous-Si (a-Si) films were sequentially deposited by plasma-enhanced chemical vapor deposition at 380 °C, followed by dehydrogenation via furnace annealing process at 450 °C. Then the a-Si films were crystallized by a 308 nm XeCl excimer laser with a line-shaped beam power of 350 mJ/cm^2. The 100 nm thick gate insulator was deposited by tetraethyl orthosilicate base oxide. Subsequently, the source/drain (S/D) regions and LDD region were defined by the mass-separated ion implanter technique. Next, the doping activation was performed by rapid thermal annealing. Finally, MoW was sputtered and patterned as a gate metal. The channel width of the TFT in this study was fixed at 10 μm and the channel length was 3 to 8 μm. The LDD length is 1.25 μm. The I-V curves are measured by a Keithley 4200 semiconductor parameter analyzer. During the stress test, the gate terminal was connected to 20 V + threshold voltage (V_t) while the S/D were grounded for 2000 s.

Figure 1 shows the normalized I_d-V_g transfer characteristics with drain voltage of 0.1 V in the LTPS TFT before and after gate bias stress. The normalized drain current is defined

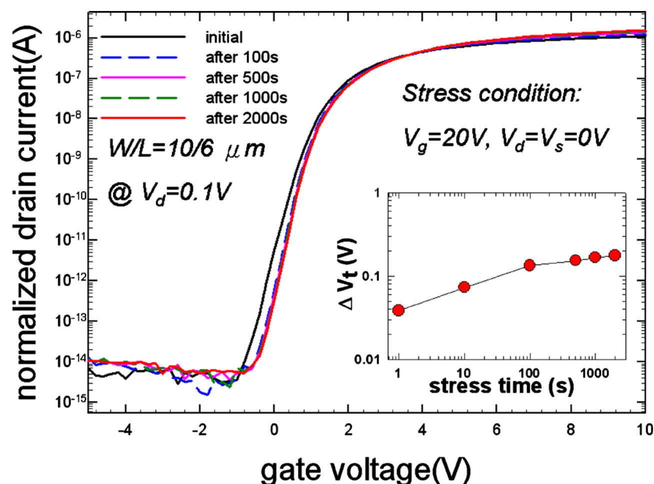

FIG. 1. (Color online) Normalized I_d-V_g transfer characteristics with drain voltage 0.1 V in LTPS TFT before and after gate bias stress; inset shows threshold voltage (V_t) with stress time.

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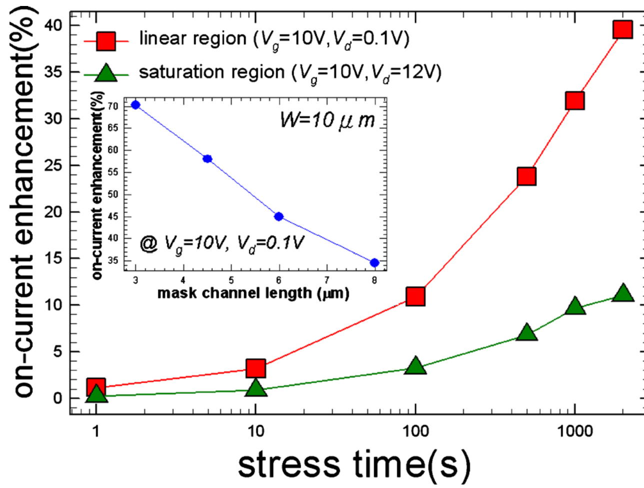

FIG. 2. (Color online) On-current (I_{on}) enhancement for linear and saturation I_d-V_g transfer characteristics with stress time; inset shows I_{on} enhancement at various channel lengths at channel width of 10 μm.

as $I_d(L/W)$. It can be seen that the threshold voltage (V_t) slightly increases after the 2000 s stress, as shown in the inset of Fig. 1. Here, V_t is defined as the gate voltage at which the drain current equals 10^{-9} A. The V_t shift is caused by the electron trapping in the gate-insulator and/or the state-creation in the channel region under the gate positive bias stress.[5,8] It is commonly known that the drain current is inversely proportional to V_t;[9] however, it can be seen from Fig. 2 that on-current (I_{on}) in both the linear and saturation regions are significantly improved after the gate bias stress.

The I_{on} enhancement in the linear and the saturation regions were extracted at V_d=0.1 and 12 V with V_g=10 V, respectively. Clearly, the I_{on} enhancement in both linear and the saturation regions increase with an increase in stress time. It is also worth noting that the I_{on} enhancement in the linear region is more evident than in the saturation region. The inset of Fig. 2 shows the I_{on} enhancement at different channel lengths at a fixed channel width of 10 μm. As can be seen, the I_{on} improvement decreases with increasing channel length. In order to better understand the mechanism of gate bias stress causing device improvement, the distribution of electric field was simulated by TCAD software.

Figure 3(a) shows the distribution of the electric field for LTPS TFTs under gate bias stress condition. As can be seen, the electric field is constant in the gate insulator with a high electrical field occurring in the gate electrode corner. In order to further examine the improvement mechanism, the distribution of electric field at the lateral coordinate (X) of 2 and 3 μm were monitored, shown as Fig. 3(b). As can be seen, the electric field at the SiO_2/gate interface for X=3 μm (the LDD region) is significantly higher than X=2 μm (the channel region), which will induce an asymmetric electric field distribution at the poly-Si/SiO_2 and the gate/SiO_2 interfaces at X=3 μm. Therefore, the strong electric field occurring at the gate/SiO_2 interface probably induces hole injection from gate electrode to SiO_2 region,[10] as depicted in Fig. 3(c). Consequently, the trapped holes in the gate-insulator induce electrons at the channel region near the edge of the LDD regions. This result causes I_{on} enhancement because the effective channel length (L_{eff}) is shortened by these accumu-

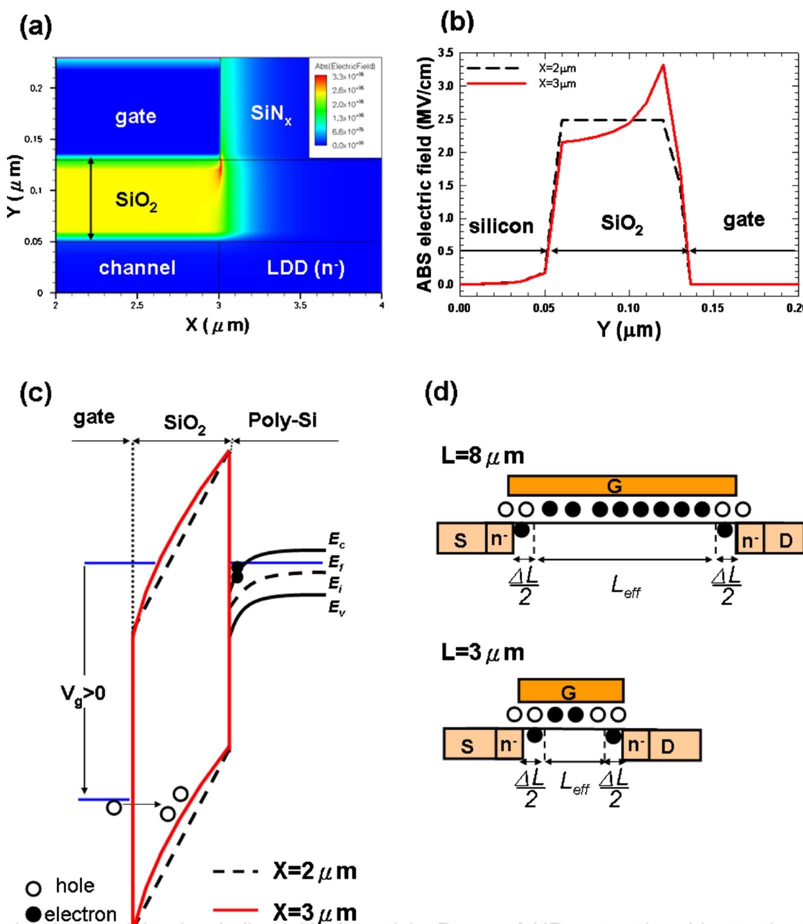

FIG. 3. (Color online) (a) Distribution of the electric field for LTPS TFT under gate bias stress condition, (b) distribution of electric field at the lateral coordinate (x) of 2 μm (dashed line) and 3 μm (solid line), (c) schematic energy band diagram for X of 2 μm (dashed line) and 3 μm (solid line) for device operating at positive voltage, (d) schematic diagram of LTPS TFTs with L=8 μm and 3 μm after gate bias stress.

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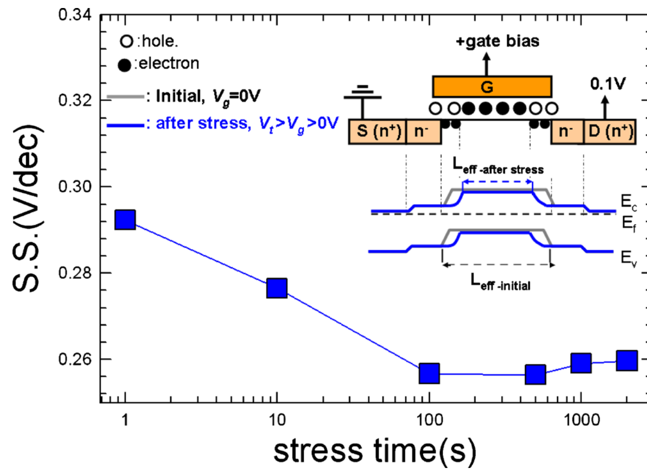

FIG. 4. (Color online) SS with stress time; inset shows schematic energy band diagram of LTPS TFTs before and after stress.

lated electrons; this is even more evident for short channel lengths than for long, as demonstrated in Fig. 3(d). The inset of Fig. 2 verifies this enhancement of I_{on}, with on-current enhancement improving is more significant in short channel length (3 μm) then in the long channel length (8 μm). It should be noted, however, that shortened L_{eff} induced I_{on} enhancement is more clearly in the linear region than the saturation region due to the generation of a pinch-off region near the drain terminal.

Figure 4 shows the SS with stress time. Here, the SS is defined as one-half of the gate voltage required to increase the threshold drain current by two orders of magnitude (from 10^{-11} to 10^{-9} A). In LTPS TFTs, the SS depends mainly on trap distribution in polysilicon film and also on the deep interface states,[11] with these trap states generally increasing during electrical stress. Nevertheless, it can be seen from Fig. 4 that the SS decreases with increasing stress time. In addition, it is well known that the SS is dominated by the diffusion current (I_{diff}) in the subthreshold region and the I_{diff} can be expressed as:[9]

$$I_{diff} \approx WqD_n \frac{N'(s) - N'(d)}{L_{eff}}, \quad (1)$$

where W is channel width, q is magnitude of electron charge, D_n is the diffusion coefficient for electron, L_{eff} is effective channel length, and N′(s) and N′(d) are the electron density per unit area at the source and drain ends, respectively. The inset of Fig. 4 shows the schematic energy band diagram of LTPS TFTs before and after stress. As can be seen, the L_{eff} significantly diminishes due to electron accumulation at the S/D edges. Consequently, the SS is also reduced after stress when the device operates at the subthreshold region.

In summary, this work investigates an improvement in anomalous on-current (I_{on}) and SS in LTPS TFTs after gate bias stress. The experimental results reveal that the improved electrical properties originate from the hole trapping at the SiO_2 above the LDD regions which reduces the effective channel length (L_{eff}). The stress-related electric field was simulated by TCAD software to verify the mechanism above. In contrast, the effects of shortened L_{eff} are not as evident at the saturation region because the pinch-off region is generated at the drain edge. Further, the SS is also diminished by the shortened L_{eff} when the device operates at the subthreshold region.

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[1]Y. C. Wu, T. C. Chang, P. T. Liu, C. S. Chen, C. H. Tu, H. W. Zan, Y. H. Tai, and C. Y. Chang, IEEE Trans. Electron Devices **52**, 2343 (2005).
[2]Y. Matsueda, R. Kakkad, Y. S. Park, H. H. Yoon, W. P. Lee, J. B. Koo, and H. K. Chung, SID Int. Symp. Digest Tech. Papers **35**, 1116 (2004).
[3]K. Yoneda, R. Yokoyama, and T. Yamada, Proceedings of Symposium on VLSI Circuits, Kyoto, Japan, 14 June 2001, pp. 85–90.
[4]H. Tokioka, M. Agari, M. Inoue, T. Yamamoto, H. Murai, and H. Nagata, SID Int. Symp. Digest Tech. Papers **32**, 280 (2001).
[5]M. Hack, A. G. Lewis, and I.-W. Wu, IEEE Trans. Electron Devices **40**, 890 (1993).
[6]Y. H. Tai, S. C. Hung, C. W. Lin, and H. L. Chiu, J. Electrochem. Soc. **154**, H611 (2007).
[7]Y. Toyota, T. Shiba, and M. Ohkura, IEEE Trans. Electron Devices **52**, 1766 (2005).
[8]F. R. Libsch and J. Kanicki, Appl. Phys. Lett. **62**, 1286 (1993).
[9]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. (Wiley, New York, 2007).
[10]H. T. Lue, E. K. Lai, S. Y. Wang, L. W. Yang, T. Yang, K. C. Chen, K. Y. Hsieh, R. Liu, and C. Y. Lu, Dig. Tech. Pap. - Symp. VLSI Technol. **2007**, 140.
[11]F. V. Farmakis, J. Brini, G. Kamarinos, and C. A. Dimitriadis, IEEE Electron Device Lett. **22**, 74 (2001).

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