行政院國家科學委員會專題研究計畫　成果報告

一種新穎絕緣層上矽動態起啟電壓金氧半元件

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一種新穎絕層上矽動態啟始電壓金氧半元件

計劃編號: NSC-91-2215-E-009-052
執行期間: 91/8/1~92/7/31

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ABSTRACT

In this study, we discuss the suppression of floating body effects by through -the-gate implantation with different implantation energy. Current drive capability, DIBL, tran -sconductance, S.S would be improved compared to control-counterpart. Both the floating body and parasitic BJT effects in PD SOI pMOSFETs were also suppressed by reduced neutral region.

1.Introduction

In recent years, the fabrication of ICs on silicon-on-insulator (SOI) MOSFET's was extremely attractive for high performance low power ULSI applications. There exist two types of SOI substrate, one is fully depleted (FD) substrate, and the other is partially depleted (PD) substrate. The PD device, due to its scalability, better threshold voltage control than the FD devices, has been the preferred candidate[1]. However, PD SOI MOSFET's have serious floating-body effects that degrade the operation of the static, dynamic, and transient device. The floating body effects were due to impact ionization. Electrons generated by impact ionization raise the n-body potential of pMOSFET's, called floating effect. The floating body effect not only reduces the threshold voltage but also lead to forward biasing of the parasitic bipolar transistor (BJT) which may cause substantial influences in the circuit performance. Therefore, the most important issue for PD SOI MOSFET's is to suppress the floating body effects for IC's design. To overcome this problem, body-tied structures, such as link-body[2], H-gate[3], and T-gate[4], were provided to conduct the carriers by impact ionization for suppressing the floating body and parasitic BJT effects. However, the floating body effects couldn't be eliminated completely, especially for SOI pMOSFET's in the above body-contact structures. This is because that large neutral region was in n-body of SOI pMOSFET's by As implantation. The doping profile would not be destroyed after RTA treatment for heavier atomic mass and low diffusion efficiency of As. In this study, the floating body and parasitic BJT effects of SOI pMOSFET's were drastically suppressed by the profile of through-the-gate implantation. By controlling the profile underneath the gate oxide precisely, the V_{TH} could be manipulated to low value, which could correspond to requirements of high speed and low power. Furthermore, Drain Induced Barrier Lowering (DIBL), Subthreshold Slope (S.S), floating body effect, parasitic BJT effect could be improved by the profile of through-the-gate implantation simultaneously.

2. Device Fabrication

P-channel MOSFETs with channel length down to 0.8μm were fabricated on 200nm 6-in p-type SOI wafers with resistivity of 15-20Ω-cm by a conventional pMOSFET process. Local oxidation of silicon (LOCOS) was used for device isolation. Wafers were then split to As channel implant for threshold voltage, $V_{TH,}$ adjustment of various implant energy and dosage. Specifically, implant energy splits were 100KeV, 250KeV, 275KeV, and the dosage splits were 5×10^{12}, 10^{13}, 5×10^{13} cm^{-2} while splits of 250KeV, 275KeV were perform after gate defined. Gate oxides thickness was 3.4nm in N_2O ambient. It should be noted here that gate dielectrics were grown by conventional horizontal furnace. Next, polysilicon (poly-Si) layer with a thickness of 200nm was deposited by low pressure chemical vapor deposition (LPCVD). The poly-Si layer was then patterned to define 0.8μm gate length. Shallow S/D extensions were formed by BF_2 implant (at 10 keV, $1\times10^{15}cm^{-2}$). After the formation of TEOS sidewall spacer (200nm), deep heavily source/drain junctions were formed by BF_2 implantation at 8 keV with a dose of 5×10^{15} cm^{-2}, and at 20 keV with a dose of 5×10^{13} for lightly source/drain junction. Finally, wafers were annealed by a rapid thermal process (RTP) at 1020□ for 20 sec for dopant activation. Afterwards, a 550nm TEOS layer was deposited and etched for contact holes. Finally, a Ti/TiN/Al-Si-Cu/TiN 4-layer mental was deposited and patterned to complete contact metallization. Electrical characterizations were performed using a HP4156 system.

3. Results And Discussion

The resultant channel doping profiles for the conventional and the ITG devices are shown schematically in Fig. 1a and 1b, respectively. It can be seen that the conventional V_{TH} adjust implant results in a medium-doped neutral region below the channel for the control device. In contrast, by using the ITG scheme, the As^+-doped region is located in the channel immediately below the gate oxide under the polysilicon gate, as well as in the bottom oxide (BOX) region under the source/drain (S/D) regions. It is worth noting here that a lightly-doped n-body region, free from the As^+-V_{TH} adjustment implantation, is preserved between the As^+-doped region and the S/D region. Fig.2 shows threshold voltage V_{TH} and subthreshold slope (S.S) versus gate length. From the left of Fig.2, Control-split has large V_{TH} while the other splits has smaller V_{TH}. This phenomenon could be attribute to the profile of doping concentration in the channel. Therefore, the doping concentration of through-the-gate splits around the channel was lower than that of the control-split. The S.S of all splits was 84mV/dec., 74mV/dec., 104mV/dec. for control, 275KeV, and 250KeV-splits respectively. The S.S of 275KeV-split was lower, about 74mV/dec., than other splits due to the reduced depletion-layer capacitance[5]. However, the S.S of 250KeV-split was close to 104mV/dec. that was to high to hardly turn off the devices. This phenomenon may be due to the depletion-layer capacitance and serious leakage current by lower threshold voltage. Drain Induced Barrier Lowering (DIBL) versus trans -conductance with V_D=1.8V was shows in Fig.3. In general, lower threshold voltage cause higher transconductance but, in contrary, DIBL would increase simultaneously. However, DIBL of 250KeV-split was below 20mV, and that of 275KeV-split was about 10mV. The doping profile by

through-the-gate implantation could drastically reduce the DIBL, and, in addition, the transconductance would increase for lower V_{TH} and higher carrier mobility due to lightly doping concentration in the channel. Next, Fig.4 shows drain voltage versus drain current at length equal to 0.8 μm with width equal to 100 μm in conventional structure. The gate voltage was started form V_{TH} to (V_{TH}-4) V. Both 250KeV and 275KeV-splits have higher driving capability for higher carrier mobility. Without body contacts in convention structure of SOI pMOSFET's, the voltage that results in floating body effects was almost the same for all split-samples. However, the parasitic BJT effect was serious in control-split due to the heavily doing concentration of the body which cause increase the bipolar gain of PNP structure. Drain voltage versus drain current in H-gate structure at length equal to 0.8 μm with width equal to 100 μm was showed in Fig.5. Driving capability was the same as that in conventional structure. The voltage that floating body effect occurred was different for all splits from the arrow in the figure. The floating body effect of control-split in H-gate structure was improved only for 0.4V. Therefore, floating body effect in SOI pMOSFETs was very serious even with body contacts. But, it was interesting that the floating body effects of 275KeV, 250KeV-splits was improved by about 2V. We believe that it is because the doping concentration by through-the-gate implantation was very light in the n-body. The neutral region was decreased for enhanced depletion region, and then floating body effect, parasitic BJT effect could both decrease simultaneously.

4.Conclusion

By through-the-gate implantation, we could reduce the threshold voltage V_{TH} to low value for 250KeV and 275KeV-splits, which could lead to enhance drain current and transconductance simultaneously due to higher carrier mobility. The doping profile by this method could also reduce DIBL, and S.S of 275KeV-split could approach to 74mV/dec. that lower than the control-split drastically. Furthermore, both floating body effect and parasitic BJT could be drastically improved because the neutral region was reduced for lightly doping concentration of through-the-gate implantation.

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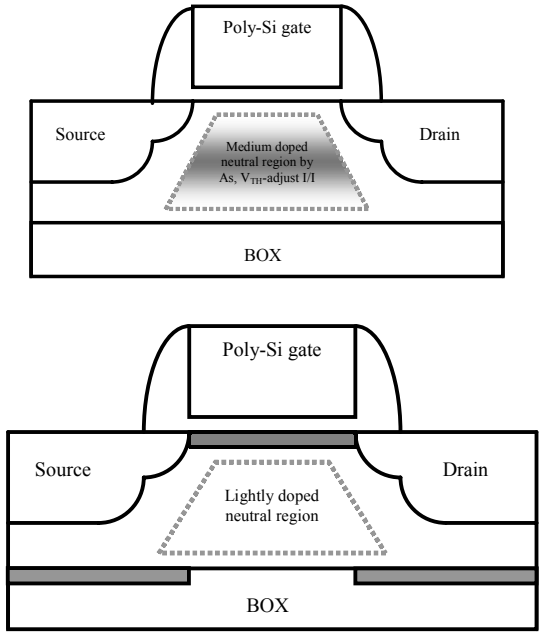

Fig. 1 Channel profiles for (a). a control device with conventional threshold adjust implant performed before the polysilicon gate is in place, and (b). a new implant-through-gate (ITG) device. Note the difference in the neutral region underneath the gate.

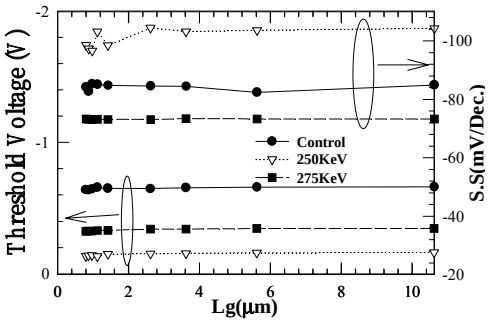

Fig. 2 Threshold voltage V_{TH} and subthreshold slope (S.S) versus gate length. The split conditions were control, 250KeV, 275KeV.

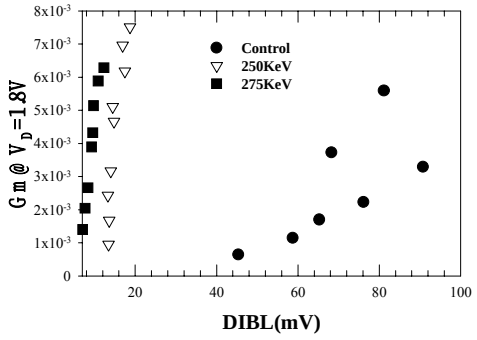

Fig. 3 DIBL versus transconductance with V_D=1.8V.

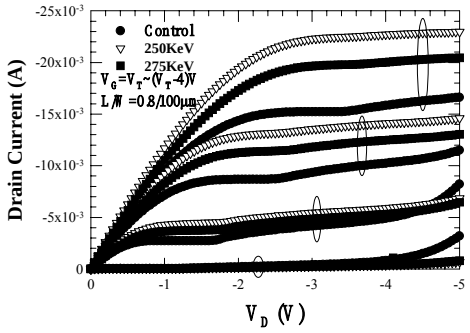

Fig. 4 Drain voltage versus drain current at length equal to 0.8 μm with width equal to 100 μm in conventional structure.

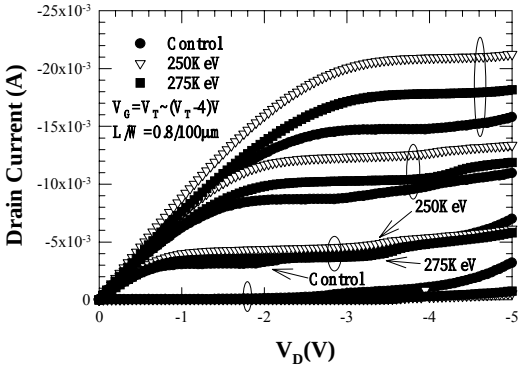

Fig. 5 Drain voltage versus drain current in H-gate structure at length equal to 0.8 μm with width equal to 100 μm