行政院國家科學委員會補助專題研究計畫成果報告

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計畫類別：▒個別型計畫　　□整合型計畫

計畫編號：NSC 89－2215－E－009－114

執行期間：89 **年** 8 **月** 1 **日至** 90 **年** 7 **月** 31 **日**

計畫主持人：陳明哲

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

□赴大陸地區出差或研習心得報告一份

□出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

執行單位：國立交通大學電子工程學系

中　華　民　國 90 **年** 10 **月** 26 **日**

行政院國家科學委員會專題研究計畫成果報告

低功率低電壓數位類比積體電路之晶片實現及設計法則(六)

Implementation and Methodology for Low Power/Low Voltage Digital and Analog Integrated Circuits(VI)

計畫編號：NSC 89－2215－E－009－114
執行期限：89 年 8 月 1 日至 90 年 7 月 31 日
主持人：陳明哲教授　　國立交通大學電子工程學系

一、中文摘要

本年度專注於5個項目：(I) **環狀震盪器及靜電放電保護電路在打線應力下之行為研究**；(II) **超薄氧化層直接穿遂對下世代**CMOS**元件電路及晶片性能影響之研究**；(III) **一種創新的射頻電感之研製**；(IV)**類比**MOSFET**之低頻雜訊研究**；**以及**(V) **磊晶層對**CMOS**靜電放電保護電路影響之研究**. **本計畫產出豐碩成果**, **並受到到國際重視**.

關鍵詞：環狀震盪器, **靜電放電輸出入**, **打線應力**, **直接穿遂**, **氧化層**, **互補式金氧半**, **射頻**, **電感**, **類比**, **雜訊**, **磊晶**.

Abstract

This year we focus our attention on 5 items ; (I) The behavior of ring oscillator and ESD protection circuit under wire bonding;
(II) The impact of oxide direct tunneling on next-generation device/circuit/chip; (III) Study of a novel RF inductance; (IV) Study of low-frequency noise in analog MOSFET; and (V) The influence of epitaxial layer on CMOS ESD protection circuit. The project has created a lot of achievements that have significantly attracted worldwide attention.

Keywords：Ring oscillator**, ESD, Bonding mechanical stress, I/O, direct tunneling, oxide, CMOS, RF, inductance, noise, analog, epitaxial layer**

二、緣由與目的

低電壓低功率消耗可攜帶型(portable)器具設備已是時勢潮流, 反映於半導體工業上無論製程技術或電路設計法則處處都可見到此潮流帶來的衝激. 國際上低電壓低功率電子(Low voltage、Low power Electronics)方面的研究一日千里進展極快。

三、研究方法與成果

(i)在 TSMC 0.13um CMOS **暨多層銅導線** /low k **介電層製程技術上設計-系列** Testkey, **包括了** ring oscillator **及** ESD **保護電路等置於** I/O pads **下以** 100%**恢復** chip **面積使用率**, **經由機械應力及電氣特性測試證實** bonding power **及** bonding force **不會造成** cracking defects **及衍生的電性劣化等**,**研究結果部份發表於** 2001 **年** IEEE EDL [1], 2001 **年** IEEE EDL [2], **及** 2001 **年** IEEE ICMTS [3]**等**.
(ii) 在 TSMC **製作一系列** testkey **包括** nMOSFET, pMOSFET,**及** CMOS inverters **等並有不同的** gate stack SiO2 **厚度**(1~3um), **以研究當** gate oxide **厚度越薄引致** direct tunneling**對下一代** device/circuit/chip **整體性能的影響及厚度極限評估**,**部份成果已發表於** 2000**年** SSDM [4], 2000**年** IEEE IEDM [5],

2000 年 IEEE T-ED [6], 2001 年 IEEE T-ED [7], 及 2001 年 IEEE T-ED [8].
(iii) 在 Winbond 製作一系列 RF testkey 主要以 inductance 為主，並提出一種創新:Floating well, 以提昇 inductance 在高頻時的性能,並已作了徹底的電性量測,分析,萃取及模擬等, 部份成果接受發表於 2001 年 IEEE T-SM [9].
(iv)在 UMC 製作一系列 MOSFET 測試鍵, 著重在 Analog 性能方面的 Low-frequency Noise 研究, 已作了徹底的長時間雜訊量測及分析,並從中發現新的現象: Dynamic percolation paths, 部份成果發表於 2001 年 JAP [10].
(v)在 TSMC 製作一系列 Epi CMOS 測試鍵以研究磊晶層 Epi layer 對 ESD 保護電路性能的影響,已作了徹底的暫態量測及創新的理論分析, 部份成果發表於 2001 年 IEEE T-ED [11].

四、結論與討論

(I) 所發表於[1] , [2] , [3]之 I/O pads 下 ring oscillator/ESD 保護電路行為之論文在國際上引起很大迴響 : Lucent /Bell Lab 及一家在 Utah 州之半導體公司 ,……等 .

(II) 所發表於 [4] , [5] , [6] , [7], [8] 探討 direct tunneling 對下世代元件電路及晶片性能影響之論文吸引國際注意，並有若干論文被引用 : Lucent/Bell Lab, IBM, Stanford University, Xilinx, IMEC, Toshiba, Hitachi, Professor Meindl's group, Singapore National University,…..等 .

(III) 所發表 [9] 之 RF 論文初步受到 Stanford University Professor Simon's group 及 Professor Lee 's group 之高度重視 .

(IV)所發表於 [10] 之類比 MOSFET 低頻雜訊論文目前已授權歐盟 IMEC 納入新編專書中 .

(V) 所發表於[11] 之 Epi CMOS ESD 論文正受國際注意如 intel, TI 等 .

五、參考文獻

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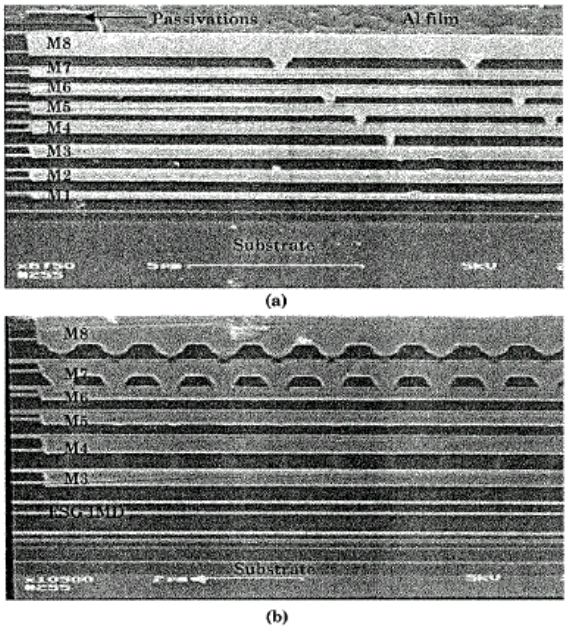


Fig. 1. SEM image of cross section of (a) a full eight-level metal I/O bond pad and (b) a six-level metal, metal-3 to metal-8, grounded-up bond pad.

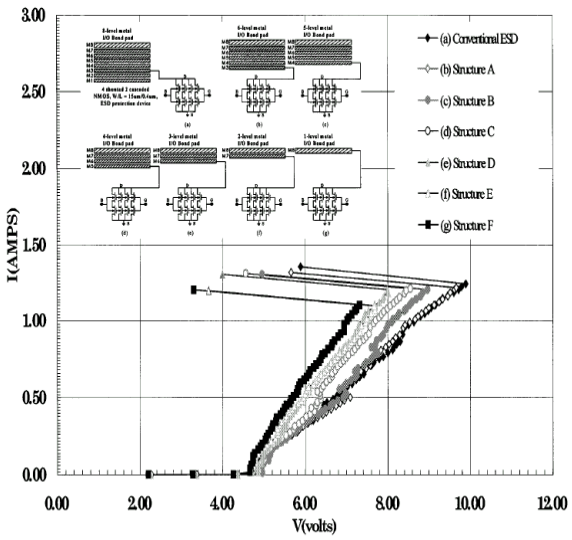


Fig. 2. *I–V* curves of the seven different structures obtained by TLP.

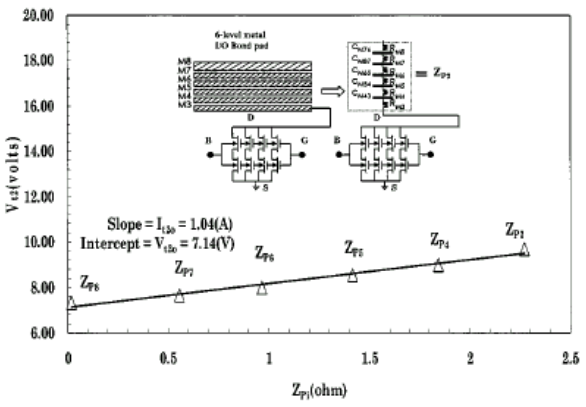
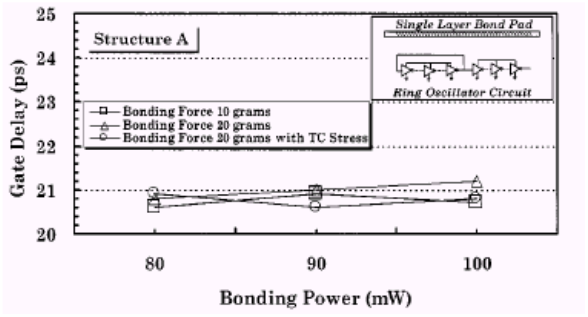
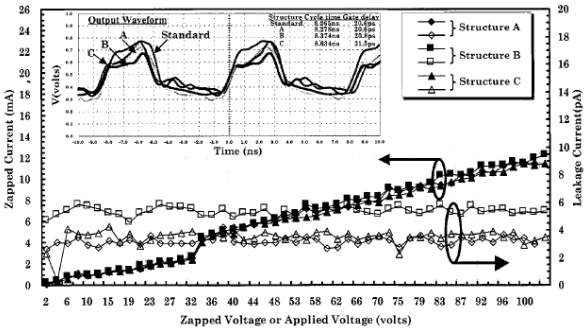


Fig. 3. Measured V_{t2} versus calculated impedance for structure A to F.





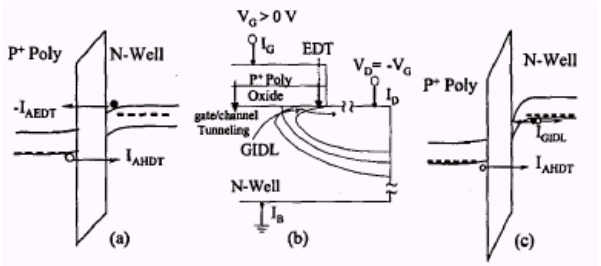
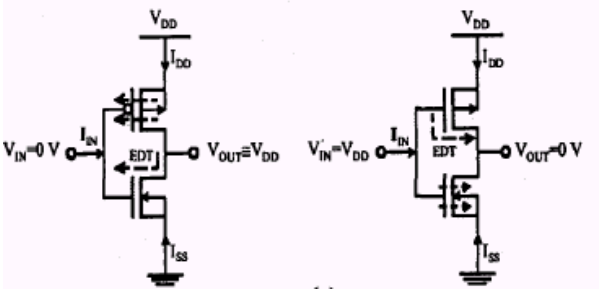


Fig. 1 (a) Band diagram located at channel region far from LDD. Accumulation hole direct tunneling current (I_{AHDT}) and electron direct tunneling (I_{AEDT}) both contribute to gate/channel tunneling. (b) Schematic cross section near gate/drain overlap region under V_G>0 V and V_D= -V_G. Three tunneling current paths are shown. (c) Band diagram located at gate/drain overlap region, showing hole EDT and GIDL.



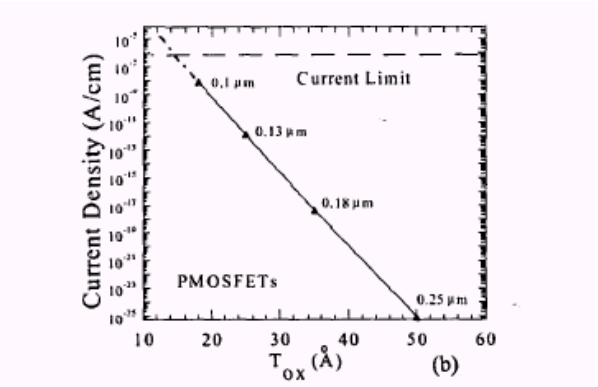
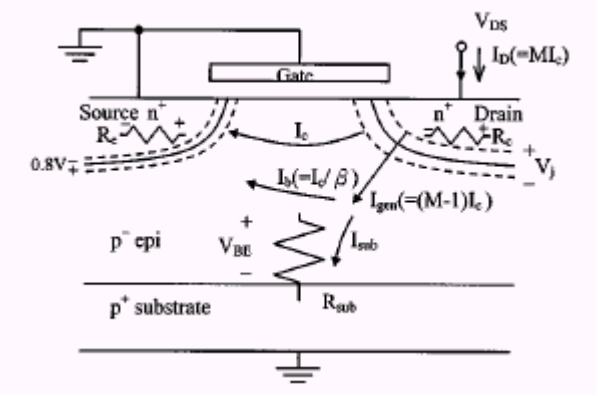


Fig. 7 (a) Showing the location of the edge hole direct tunneling. (b) The calculated hole direct tunneling per gate width versus scaling generation oxide thickness in PMOSFETs.



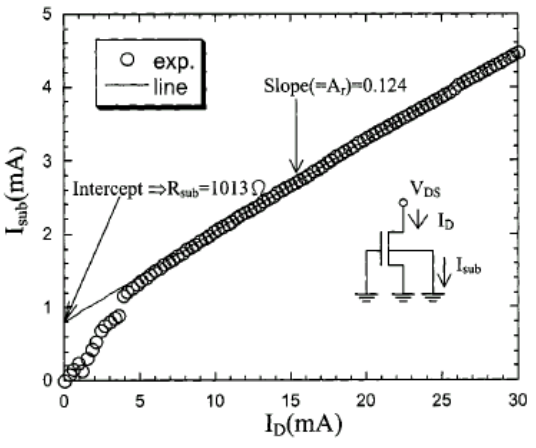


Fig. 2. Scatter plot between measured substrate current and drain current. A straight line fitting data points for $I_D > 4$ mA is drawn. The inset depicts the test configuration.

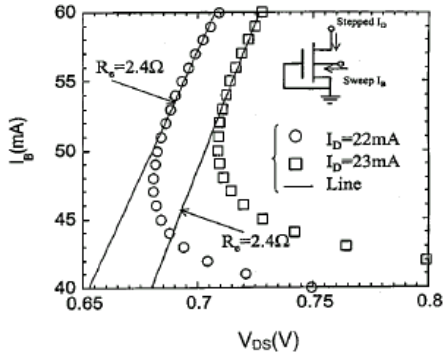


Fig. 4. Set-up of extracting the emitter series resistance as well as the measurement results.

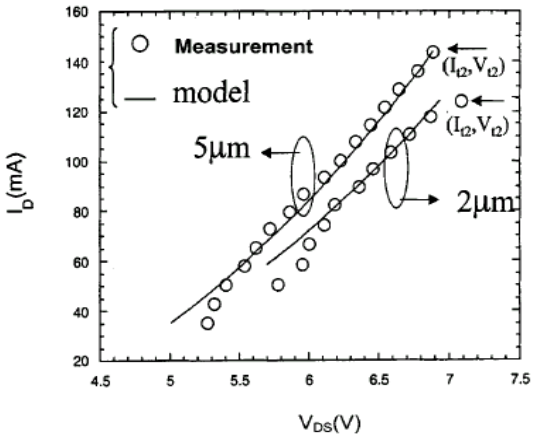


Fig. 10. Experimental I–V characteristics and calculated results for high-level injection current gain model. $R_e = R_c = 3.1\ \Omega$ for epitaxial layer thickness of 2 μm and $R_e = R_c = 2.1\ \Omega$ for 5 μm.

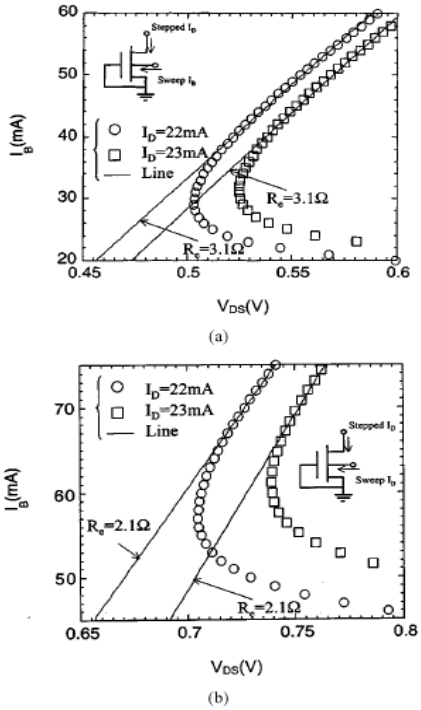


Fig. 11. I–V of extracting the emitter series resistance for structures having epitaxial layer thickness of (a) 2μm and (b) 5 μm.

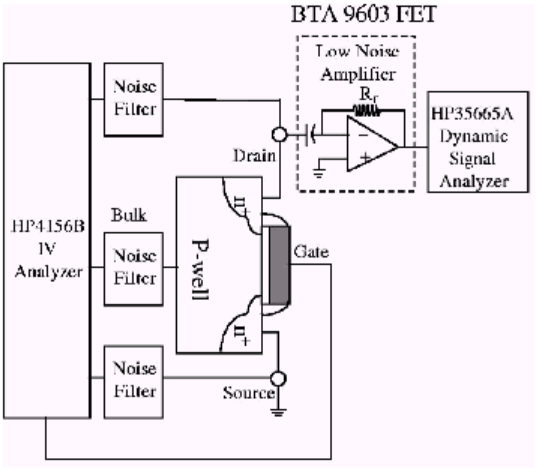


FIG. 1. Schematic diagram of the drain current noise measurement system.

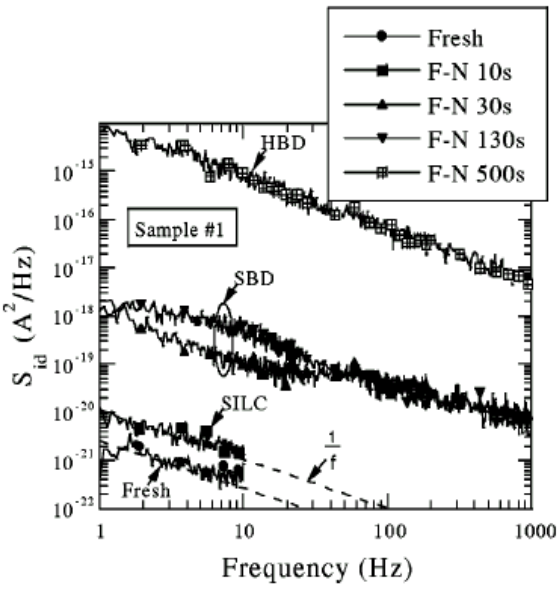


FIG. 6. Measured drain current noise spectra (S_{id}) with V_D=0.1 V and V_G=1 V for several stress times.

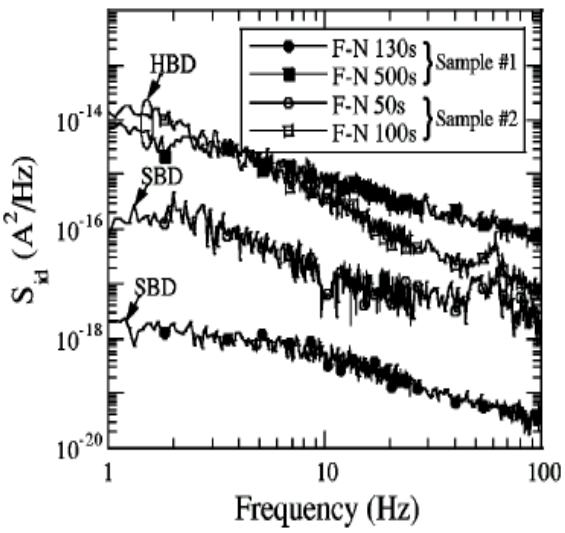


FIG. 11. Comparisons of the measured S_{id} under the bias condition of V_D =0.1 V and V_G=1 V in the first SBD and the final HBD for two samples.