行政院國家科學委員會專題研究計畫成果報告

一新型之電荷幫浦鎖相迴路
A New Charge-Pumped Phase-Locked Loop

計畫編號: NSC89-2215-E-009-116
執行期限: 89年8月1日至90年7月31日

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一、中文摘要(關鍵詞:鎖相迴路，電荷幫浦)

本研究計畫的目的是提出一個新型的電荷幫浦鎖相迴路，以縮短其拉進(pull-in)及鎖定(lock-in)時間而不致造成電壓控制震盪器(VCO)輸出信號頻率的不穩定、相位擺動大及VCO的過載。因此本計畫內容含有：（1）提出此新型鎖相迴路；（2）以電腦模擬來驗證此鎖相迴路的優越特性；（3）提出一實現此鎖相迴路之電路架構與線路。

Abstract

Keywords: Phase-Locked Loop, Charge Pump

This proposal presents a new charge pump PLL which modulates the charge pump current magnitude and constrains constant voltage jump in voltage-controlled oscillator (VCO) input. Hence the new PLL can reduce the pull-in and lock-in time as well as avoid frequency jittering enlargement and VCO overload. One realization is included. Simulations are conducted to verify the usefulness of the new PLL.

二、緣由與目的

Charge pump PLLs are widely used for synchronization in communication receivers [1]. The block diagram shown in Fig. 1 is a charge pump PLL which consists of four function blocks: a three-state phase detector, a charge pump, a R-C loop filter, and a VCO. The outputs, V_u, V_d, of the three-state phase detector allow only three different states, $(V_u = 1, V_d = 0), (V_u = 0, V_d = 1)$, and $(V_u = 0, V_d = 0)$, which are used to control switches, S_1, S_2, in the charge pump. The duration of each state is proportional to the phase difference between the input signal, V_i, and the VCO output, V_o. The loop filter may be charged, discharged, or neutral, corresponding to the three states, respectively. Then, the loop filter output, V_f, controls VCO output to track the oscillating input signal.

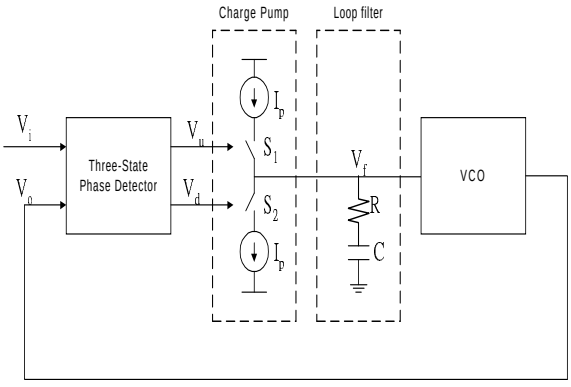

圖 1: Block diagram of the charge pump PLL

To increase the response speed, existing approaches[3, 4] modulates the magnitude I_p of

charge pump current proportional to the phase difference. While the increasing current magnitude reduces the pull-in and lock-in time, the voltage jump, I_pR, in VCO input also increases, resulting in larger frequency jittering which is not allowed in some applications [1]. Further, large voltage jump also may overload the VCO [2]. In this proposal, we propose a new charge pump PLL which not only modulates the charge pump current but also constrains constant voltage across the resistor. Hence, the new PLL can both reduce the pull-in time and avoid the large voltage jump in the VCO input. We also present a realization and simulation results to verify the usefulness of the new PLL.

三、研究方法及成果

1 Stability and VCO Overload

Since the charge pump PLL is a closed-loop system, it may be unstable. Such a system is nonlinear and its exact response can be computed by iteratively solving nonlinear equations [2]. General stability analysis of such system is difficult; however, the linearization approach is often taken to derive the condition for PLL to be stable [1, 2]:

$$I_pRK_vT < \frac{2}{1+\frac{T}{2RC}} \tag{1}$$

where K_v is the VCO gain and T is the period of input V_i.

Practical VCO has limited range of its oscillating frequencies; thus VCO input voltage is constrained. To avoid VCO overload, the constraint is derived in [2],

$$I_pR < \frac{1}{K_vT} \tag{2}$$

It is also known [1] that the voltage jump, I_pR, results in frequency excursion. Hence, increasing charge pump current yields increasing voltage jump in the VCO input, resulting in increasing frequency jittering.

Define

$$f_N = \frac{T}{2\pi}\sqrt{\frac{K_vI_p}{C}} \tag{3}$$

$$\xi = \frac{R}{2}\sqrt{K_vI_pC} \tag{4}$$

where f_N is called the normalized frequency and ξ the damping factor. Then the stability condition (1) and VCO overload constraint (2) can be expressed in terms of f_N and ξ,

$$\begin{array}{ll} \text{Stability condition:} & f_N < \frac{\sqrt{1+\xi^2}-\xi}{\pi} \\ \text{VCO overload constraint:} & f_N < \frac{1}{4\pi\xi} \end{array} \tag{5}$$

The above two constraints are shown in Fig. 2. The intersected area below the curves is the allowable operating region under the stability and VCO overload constraints. It is observed that two curves are crossed at $\xi = 1/(2\sqrt{2}) \simeq 0.35$. Hence, as shown in the figure the VCO overload constraint dominates when $\xi > 0.35$. Since most practical PLL chooses $\xi > 0.4$ to avoid large overshoot, VCO overload constraint is the dominant factor in designing a PLL.

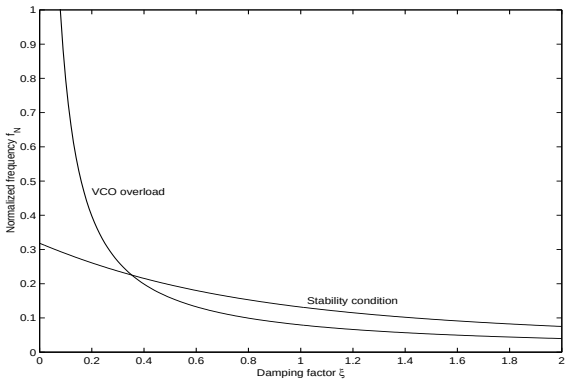

圖 2: Stability condition and VCO overload constraint in terms of ξ and f_N

2 New Charge Pump PLL

The proposed PLL satisfies the following two relations:

$$I_pR = V \tag{6}$$

$$I_p = \begin{cases} I_{min} + (I_{max} - I_{min})\text{sgn}\tau & \text{during } \tau \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

Where V is a constant chosen not to overload the VCO and τ is the time interval proportional to the phase difference. The sign of τ is positive (negative) when the input signal leads (lags) the VCO output. Note that while the current modulation

is identical to that in [4], the first constraint (6) further increases the pull-in speed and avoids VCO overload and frequency jittering enlargement.

The PLL can be realized in several ways. One straightforward realization is to adjust the charge pump current magnitude and the resistor value in the loop filter according to (6,7). Since I_pR is a constant, the voltage drop of resistor can be $V, -V$, or 0 when the charge pump is charging, discharging, or neutral. Hence, the resistor can be replaced by constant voltage supplies and switches controlled

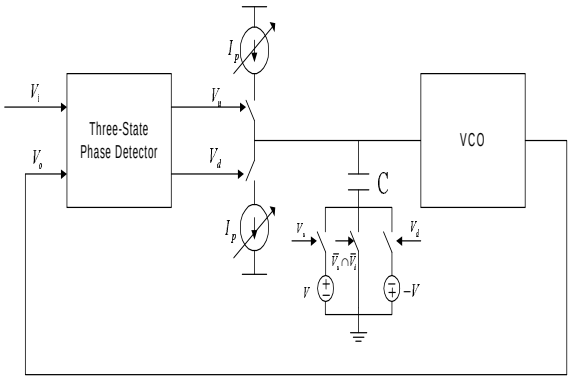

圖 3: One realization of presented charge pump PLL

The I_{max} and I_{min} can be designed as follows: Substituting (6) into (4) and rearranging yield

$$\xi = \frac{V}{2}\sqrt{\frac{K_v C}{I_p}} \tag{8}$$

Since V, K_v, and C are constants, one positive I_p uniquely gives one ξ. Hence, the PLL design can be thought of adjusting the damping factor in an interval $[\xi_{min}, \xi_{max}]$, for example $[0.4, 1]$, according to the phase difference. The values of I_{max} and I_{min} are obtained by solving (8) for the damping factors ξ_{min} and ξ_{max}, respectively.

The analysis technique proposed in [2] is extended to analyze the new PLL. Simulation results are shown in Fig. 4 which demonstrates the transient behaviour for the phase step and frequency step inputs for $\xi_{min} = 0.4, \xi_{max} = 0.707$ and $F_N = 0.1$. It is observed that the new charge pump PLL has faster transient response, as expected.

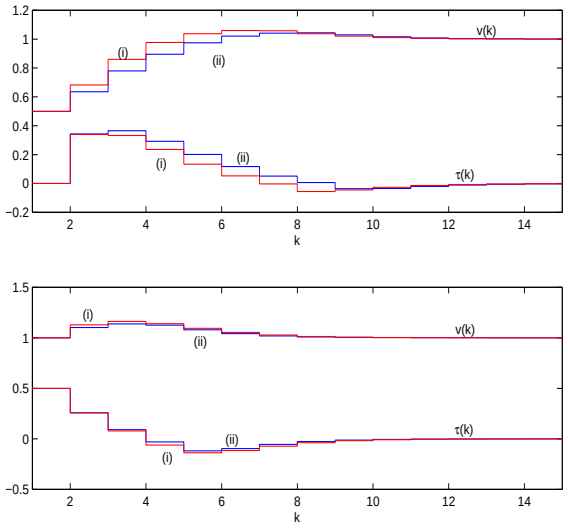

圖 4: Simulation Results for (i) New PLL: $F_N = 0.1, \xi_{min} = 0.4, \xi_{max} = 0.7$; (ii) Conventional PLL: $F_N = 0.1, \xi_{min} = \xi_{max} = 0.7$.

四、結論與討論 In this proposal, we present a new charge pump PLL which not only modulates the charge pump current but also constrains the constant voltage drop across the resistor in the loop filter. The modulated current increases the pull-in speed; further the constant voltage jump in VCO input avoids VCO overload and frequency jittering enlargement. One realization is given and simulations are also done to verify the usefulness of the new PLL.

五、計畫成果自評

本計畫研究與原計畫內容相符合，也達成原計畫中所預期的目標－提出一個新型的電荷幫浦鎖相迴路，以縮短其拉進(pull-in)及鎖定(lock-in)時間而不致造成電壓控制震盪器(VCO)輸出信號頻率的不穩定、相位擺動大及VCO的過載。我們目前正整理結果以寄出發表。綜合而言，我認為此計畫執行成果達到預期目標，為一成功的計畫。

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