行政院國家科學委員會專題研究計畫成果報告

低功率低電壓數位類比積體電路之晶片實現及設計法則(IV)

Implementation and Methodology for Low Power/Low Voltage Digital and Analog Integrated Circuits(IV)

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一、中文摘要

本計劃承襲我們以往於低功率低電壓積體電路領域之研究成果，繼續作更深入完善之研究。進行的項目是：(1)根據閘控橫向雙載子結構及背閘技術製作新式記憶細胞晶片之實現、測試及設計法則；(2)背閘2態控制臨界電壓之新式數位電路以環振盪晶片盪式實現、測試及設計法則；(3)混合式積體電路中低功率低電壓取樣保存電路晶片之實存研究及設計法則；(4)提高電路品質的新式匹配改善技巧及解析設計模式；(5)次臨界互補式金氧半基本類比計算及電壓參考源晶片之製作、測試及設計法則；及(6)閘控雙載子及互補式金氧半元件雜訊量測分析。本計劃產生之成果除以論文專利及實作展示顯現外，對於國內半導體工業在此一低功率低電壓嶄新領域之發展將有極大助益。

關鍵詞：低功率，低電壓，記憶體，數位類比，積體電路，混合式，次臨界，匹配，可攜帶型，雜訊

Abstract

As highlighted by the research achievements over the three years, this project has extensively investigated the low power/low voltage integrated circuits. The topics performed are: (1) implementation, measurement, and design methodology of the novel memory chip based on a high-gain gated lateral BJT structure as well as on a back-gate bias technique; (2) chip implementation, measurement and design methodology of new digital circuits in terms of a ring oscillator by means of back-gate controlled dynamic threshold voltage; (3) experimental study and design methodology of sample/hold chips for low power/low voltage mixed mode IC; (4) new match improvement techniques and analytic design model for enhanced circuit quality; (5) basic analog computation circuits and voltage references utilizing subthreshold CMOS; and (6) Noise characterization and analysis of gated BJTs and CMOS. The achievements created from the project will be demonstrated in terms of paper, patent, and also practical show. In addition, our work will be a great aid to our semiconductor industry in the new field of low power/low voltage integrated circuits.

Keywords: Low power, Low voltage, memory, digital-analog, IC, mixed-mode, subthreshold, match, portable, noise

二、緣由與目的

低電壓低功率消耗可攜帶型(portable)器具設備已是時勢潮流，反映於半導體工業上無論製程技術或電路設計法則處處都可見到此潮流帶來的衝激。國際上低電壓低功率電子(Low voltage、Low power Electronics)方面的研究一日千里進展極里。

研究方法與成果

(i)一里新式 SRAM 記憶胞 cell(此R 在 CMOS 製程相容下，應用高電流增益開控橫向雙載子電晶體之特性在低電源電壓下就可就 base current(基極電流)逆向現象，利用此現象以實存證明具有 SRAM cell 性能，卻僅需二個 MOSFETs 元件即可，比傳統邊式大幅降低消耗之面積)，亦獲就中華民國及民國專利。

(ii)一里 2 態 (dynamic) 臨界電壓 (threshold voltage) 技巧 (在數位 switching 時 active，將 back-gate 民以 slightly forward biased 民在 stand-by 時則 back-gate 民以 reverse bias，民此就可在訊民變化時增加充電或放電電流，且在 stand-by 時可保且 off-current 最小值以降低 stand-by power；R 實現低電壓低功率數位電路之有值方法之一)，亦獲就民國及中華民國專利。

(iii)一里類比開關(Analog Switch)或 Sample-and-Hold(取樣保存)(低電壓低功率 Analog Switch 或 Sample/Hold 亦是 mixed IC 關鍵部份，我們亦已發展出新式補償電路技術以克服 charge injection 電荷注入)。

(iv)一里改進match匹配技巧(我們已發展出以 back-gate slightly forward biased 技巧即可改進低電壓數位及類比電路之元件匹配能注，此R CMOS 製程相容，並無引引Latch-up 鎖定或干擾之疑慮)。

四、結論與討論

產出重要成果民下:

1. 發要4要IEEE DD 1要IEEE EDL，2要IEEE JSSC，1要IEEE Trans. CAS，1要IEEE Trans. CAD of ICAS，1要IEEE Trans. Semiconductor ManufacturingD
2. 獲就6項ROC專利及3項US專利D
3. 一要論文[4]] 引用於 1997 Proceedings of the IEEE(Special Issue on nanometer-scale science & technology);
4. 我們已成功以 back-gate bias 技巧應用& n-cell flash memory & 就 low voltage, low power, high reliability flash memory 成R 可能. 已建立完整實存數據,有部分具世界水水,撰論文投稿[22]。
5. 在 back-gate bias 技巧方面,我們已成功分稿出二里不同的 band-to-band tunneling 成份(一R surface,一R 同下 bulk)。
6. mismatch 除同 transistor 外，capacitor 亦同重要.我們已同 TSMC 就 0.35μm mixed-mode process 進行合作，開發成功 IPO(inter-poly oxide) capacitor,並獲 TSMC 強烈優先推薦 USA patent。目薦已有一要論文] IEEE EDL[20]接受。
7. 一里新受補償電荷注入技巧(US patent 5479121),已] 工研院微電子部門引用研發成功視訊類比數位轉換器。
8. 獲就1996年宏碁龍騰博士論文獎(獎導學生何繼助博士論文)。
9. 已創新一里測試鍵可萃取連接導線寄生電容，電阻及線寬等。已成功預測環振盪器速度之製程變化值[19]。
10. Mismatch 量測 data 已順利推進 0.15μm 製程並已建立新的統計模式。

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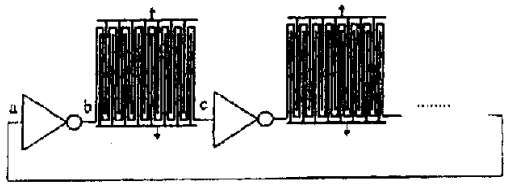
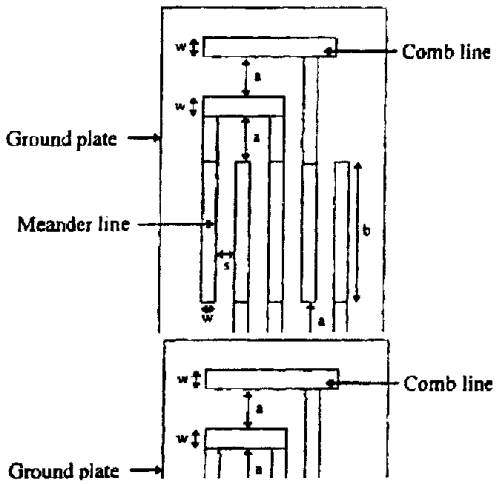
圖表



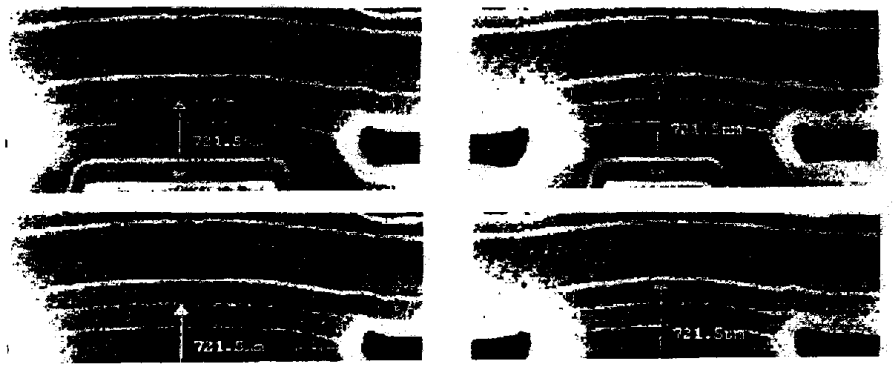
ring oscillation with wire loading



Top view and cross section of interconnect parasitic test structure

TABLE I
COMPARISON OF THE NEW METHOD AND SEM

Inter-metal dielectric thickness				
Width (μm)	Space (μm)	Cross Section	SEM (Å)	New Method (Å)
0.75	0.75		10400	10864
0.75	14.0		6000	5679



Dielectric thickness variation versus metal wire width (a)1.5um (b)0.8um