行政院國家科學委員會研究計畫成果報告

計畫題目: BESOI的新製程

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一、 中文摘要

我們利用氧電漿的處理來增進低溫的晶片黏著製程。以這種方法處理的優點在晶片黏著技術可以在600 ℃下完成，幾乎不會有硼元素從蝕刻終止層外擴散的問題。就如同掃瞄式電子顯微鏡所觀察到的結果，若將兩片以此製程黏好的晶片用力撬開，我們發現兩片晶片分開處是在於矽-氧化層的介面而非原本相黏的氧化層-氧化層介面。反觀若在600 ℃下黏著而沒有用氧電漿處理的話，根本不會有黏著的現象，除非將黏著溫度升到1100 ℃。由穿透式電子顯微鏡的觀察我們發現黏著的介面具有非常好的結構完整性。從電容量測得知黏著後的氧化層其氧化層電荷密度為-2.0×10^{10}，這樣低的電荷密度非常適合用於絕緣層上有矽的應用。

關鍵詞：黏著並回蝕的絕緣層上有矽，氧電漿處理，高速元件

Abstract

We report a oxygen plasma enhanced low-temperature wafer bonding process. At a thermal bonding temperature of 600 °C, there is negligible boron out-diffusion from the etch-stop layer. As observed by cross-sectional Scan Electron Microscopy, the bonding strength of oxygen plasma treated sample is so large that forced break from bonded wafers separates the oxide-Si hetero-interface instead of the oxide-oxide bonding interface. In sharp contrast, there is no chemical bonding for samples by the same 600 °C anneal but without oxygen plasma treatment. Such strong bonding is theoretically not possible in conventional process until the annealing temperature reaches 1100°C. The bonded interface shows good structure integrity as observed by cross-sectional Transmission Electron Microscopy. A low oxide charge density of -2.0×10^{10} cm^{-2} is obtained from capacitance-voltage measurement. The plasma induced charges during this bonding process are very low that is suitable for SOI applications.

This paper has been submitted to Appl. Phys. Lett.

Keywords: BESOI, oxygen plasma treatment, high-speed devices

二、 緣由與目的

Silicon-on-insulator (SOI)[1,2] has attracted much attention recently because of the application in low-power high-performance CMOS devices, power devices, and micro-mechanical structures. The bond and etchback SOI (BESOI)[3-5] is a promising technique to fabricate SOI, and the thick oxide in BESOI is especially useful for high speed devices and power devices. The process of BESOI bonds two oxide surfaces grown on each silicon wafers, and a selective etch-stop process is followed to remove one of the substrate and leaves less than 0.1μm Si layer on the bonded oxide. The bonding surfaces of oxide are hydrophilized and brought into contact at room temperature. Initial contact is performed by applying gentle pressure at some location on the pairs. Permanent bonding is then achieved by annealing at elevated temperatures (~1100°C), that is necessary to increase the bonding strength for device fabrication. Unfortunately, the high temperature bonding process creates some drawbacks. Boron (B) dopant in selective etch-stop layer will diffuse into active Si and buried oxide during the required high temperature process. The diffused B will cause a threshold voltage shift in a MOSFET and is unacceptable for circuit application. Although a high temperature hydrogen anneal can reduce the B concentration in active Si layer,[6] a high concentration of B is still left in the buried oxide and will diffuse out by subsequent thermal cycle used for device fabrication.

In this letter, we proposed a new bonding process to overcome this problem. A low temperature of 600 °C is used to lower the thermal budget, and there is negligible B out-diffusion at this temperature.[7,8] In order to enhance the bonding energy, we have used O_2 plasma treatment to increase the activity of bonding interfaces.[9,10] It has been reported by Sun et al.[9] that plasma treatment enhances the number of OH-groups at surface by an order of magnitude, and the increased OH-groups improves wafer bonding. Farrens et al.[11] also reported that plasma induced surface charges enhance the growth rate of oxide at the bonding interface, which is due to increased atom mobility in the near-surface region and reduced free energy of oxide formation by radical reactant ions.

三、 實驗方法

Standard 4-in. (100) silicon wafers were used in this experiment. Wet oxides of 1100 Å were grown on each wafer at 850°C. Standard RCA cleaning process is used to achieve a hydrophilic condition. One set of wafer was treated with oxygen plasma of 50 W and 20-sccm-flow rate for 4 minutes, and then followed by an initial contact. Another set was performed with initial contact directly. Thermal bonding was performed at 600 °C in nitrogen ambient for 15 hours. Cross-sectional Scan Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), were used to examine the material properties after wafer bonding. MOS capacitor was fabricated by Aluminum (Al) metalization and capacitance-voltage (C-V) measurements were used to characterize the electrical properties of bonding interface.

四、 結果與討論

In order to investigate the effect of oxygen plasma treatment, the bonded wafers were forced to break from the bonding interface. Fig. 1 shows the cross-sectional SEM of the broken wafer from the bonding interface, without the oxygen plasma treatment. The measured oxide thickness is 1160 Å, which is close to the original oxide thickness before bonding and within experimental error. The forced broken wafer shows the same violet color before bonding and throughout the whole surface. This is an indication that there is no chemical reaction after 600 °C thermal treatment. This is in consistent with reported paper in literature that a high temperature of ~1100 °C is required to form strong chemical bonding.

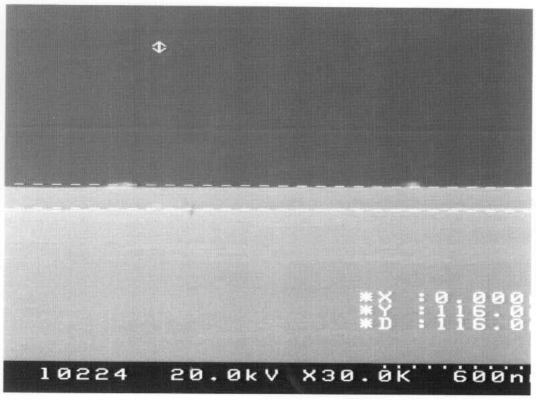
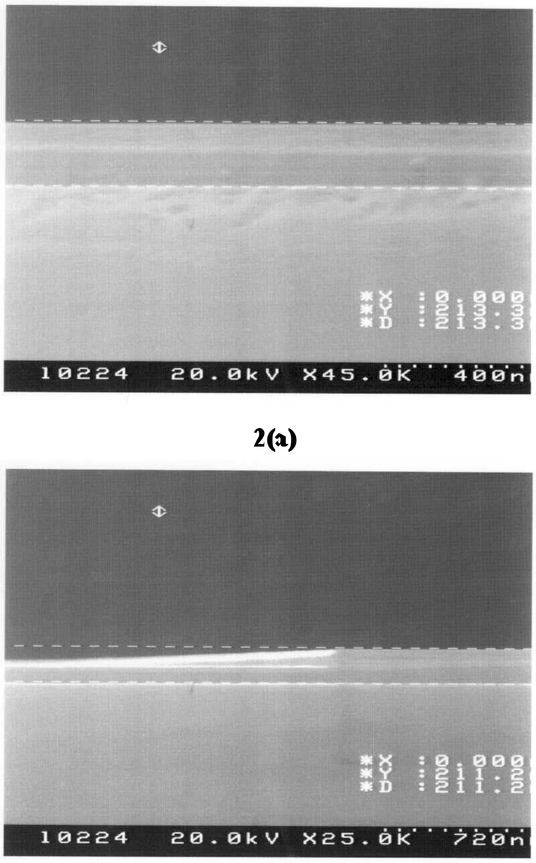


Fig. 1. Cross-sectional SEM of bonded wafer by forced break. The bonding conditions are 600 °C thermal annealing for 15 hours.

The bonding interface of oxygen plasma treated wafer, after forced to break, is shown in Fig. 2(a). In sharp contrast to the one without oxygen plasma treatment, the measured oxide thickness is 2130 Å, which is the double thickness of initial oxide thickness. A thin white line of ~ 150 Å is observed in the middle of oxide that may be the bonding interface after oxygen plasma treatment. To further demonstrate the above assumption, we have also examined the cross-sectional SEM in an air-bubbled region. As shown in Fig. 2(b), the oxide thickness is gradually decreased from bonded region into air-bubbled region, and a clear bonding interface is observed. The thickness difference between bonded region and air-bubbled region is about twice which is a strong evidence of successful bonding by oxygen plasma treatment. It is noted that the bonding strength is so large in the oxide-oxide-bonding interface that did not separate after forced break. Instead, the separation is taken place at oxide-Si hetero-interface. As observed by microscope, the thermally grown oxide of one wafer is stripped off and attach to the oxide of another wafer after forced break. Such strong bonding can only be obtained by conventional method after a high temperature annealing at ~1100 °C where a viscous flow of oxide takes place at this temperature.[4]

We have used cross-sectional TEM to further study the oxygen plasma treated bonding interface. As shown in Fig. 3, there is no defect in bonded oxide that can be observed by cross-sectional TEM.



2(a)

2(b)

Fig. 2. Cross-sectional SEM of bonded wafer by forced break in (a) bonded region and (b) air-bubbled region. Oxygen plasma treatment is used before thermal annealing.

Furthermore, in spite of the bonding interface, there is another interface that is also observed beneath the bonding interface. The separation of these two interfaces is ~ 150Å that may be due to the oxygen plasma treatment. Although the detailed mechanism of oxygen plasma treatment is not well known, the high-energy plasma may damage the oxide to break the Si-oxide bonds and create traps. It may also form oxygen-rich oxide after oxygen plasma treatment. Therefore the ~ 150 Å region, beneath bonding interface, may be due to the newly formed oxygen-rich oxide after oxygen plasma treatment.

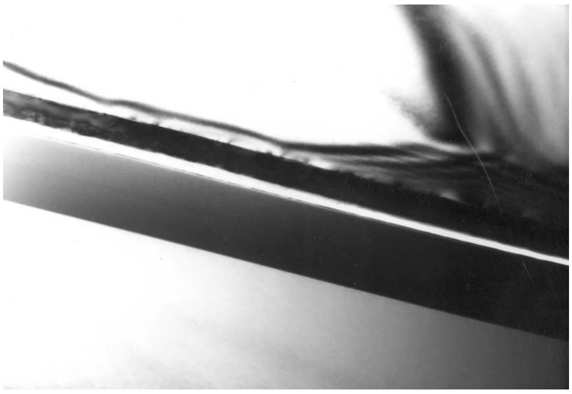


Fig. 3. Cross-section TEM of the bonding interface after forced break.

To further characterize the electrical properties of oxygen plasma treated bonding interface, we have fabricated MOS capacitor on these oxides shown in Fig. 2(a) and after forced break. Fig. 4 shows the measure C-V and an effective oxide charge density of -2.0E10 cm^{-2} is obtained. In contrast to the normally observed positive charge density, the measured negative charge may be due to trapped electrons from plasma or dangling bonds broken by oxygen plasma. Other possibilities may be due to over-saturation of hydrogen in oxide by hydrophilic bonding surface proposed by Afanas'ev et al.[5]

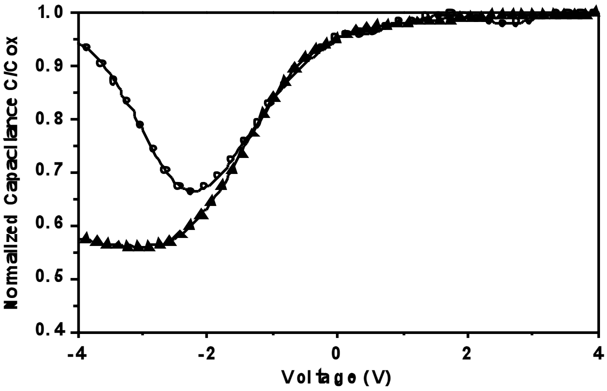


Fig. 4. C-V curve of the bonded oxide.

It is noted that this negative charged oxide can be easily repaired and converted into normal positive charged oxide by grown a very thin oxide of 50 Å. Fig. 5 shows the measured C-V curve and an effective oxide charge density of 6.6E10 cm^{-2} is obtained. In spite of the negative value, the density of effective oxide charge is quite low that demonstrates good electrical quality and is suitable for SOI application.

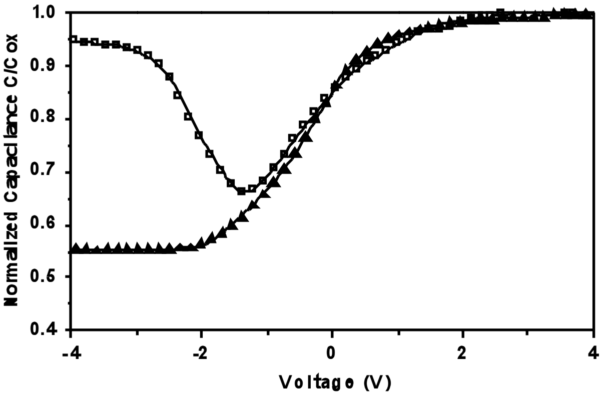


Fig. 5. C-V curve of the bonded oxide after grown 50Å thermal oxide.

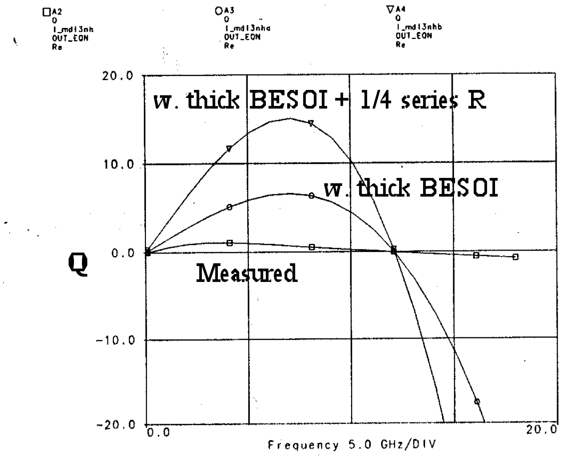


Fig. 6. Improvement of effective quality factor Q of 3-nH inductor as using thick oxide in BESOI and reducing resistance.

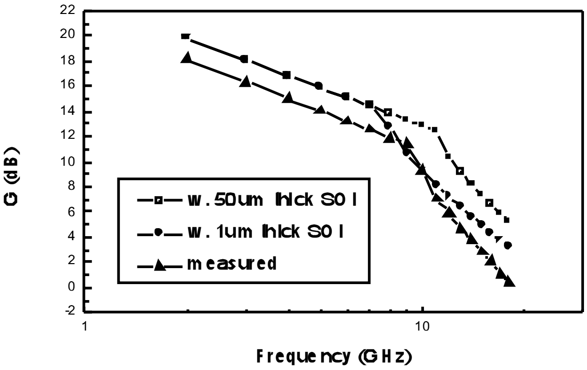


Fig. 7. Improved oxide gain of quarter-mm MOSFETs as a function of oxide thickness in BESOI.

五、 結論

We have demonstrated an oxygen plasma enhanced low-temperature wafer bonding process. The bonding strength of oxygen plasma treated sample is so large that separates the oxide-Si hetero-interface after forced break instead of the oxide-oxide-bonding interface. In sharp contrast, there is no chemical bonding for samples by the same 600 °C anneal but without oxygen plasma treatment. Such strong bonding is theoretically not possible in conventional process until the annealing temperature reaches 1100 °C. The plasma-induced charges during this bonding process are kept very low that is suitable for SOI applications.

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六、 參考文獻

[1] P. C. Yang and S. S. Li, Appl. Phys. Lett. 61, 1408 (1992).

[2] H. S. Chen and S. S. Li, IEEE Trans. Electron Devices 39, 1740 (1992).

[3] J. B. Lasky, Appl. Phys. Lett. 48, 78 (1986).

[4] W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, J. Appl. Phys. 64, 4943 (1988).

[5] M. Shimbo, K. Furukawa, K. Fukuda, and K. Tanzawa, J. Appl. Phys. 60, 2987 (1986).

[6] N. Sato and T. Yonehara, Appl. Phys. Lett. 65, 1924 (1994).

[7] W. E. Beadle, J. C. C. Tsai and R. D. Plummer, Quick Reference Manual for Silicon Integrated Circuit Technologies, John Wiley & Sons, 1984.

[8] A. Chin, K. Lee, Y.-C. Huang, Y.-S. Lin, and W. Hsu, Proceedings of Micro System Technologies, 223, Germany (1996).

[9] G.L.Sun, J.Zhan, Q.Y.Tong, S.J.Xie, Y.M.Cai, and S.J.Lu, J. Phys. C. 49, 79 (1988).

[10] G.Kissinger, and W.Kissinger, Sensors and Actuators A, 36,149 (1993).

[11] S.N.Farrens, J.R.Dekker, J.K.Smith, and B.E.Roberds, J. Electrochem. Soc., 142, 3949 (1995).

[12] W. P. Maszara, J. Electrochem. Soc. 138, 341 (1991).

[13] V.Afanas'ev, P.Ericsson, S.Bengtsson, and M. O. Andersson, Appl. Phys. Lett. 66, 1653 (1995).