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Reduction of photoleakage current in polycrystalline silicon thin-film transistor using NH_3 plasma treatment on buffer layer

Hau-Yan Lu,[1] Ting-Chang Chang,[2,a)] Po-Tsun Liu,[3] Hung-Wei Li,[1] Chin-Wei Hu,[4] Kun-Chin Lin,[4] Chao-Chun Wang,[1] Ya-Hsiang Tai,[3] and Sien Chi[1]
[1]*Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, Taiwan 300, Republic of China*
[2]*Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-sen University, 70 Lien-hai Road, Kaohsiung 804, Taiwan, Republic of China*
[3]*Department of Photonics and Display Institute, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsinchu, Taiwan 300, Republic of China*
[4]*LTPS Array Process Department, AU Optronics Corporation, Hsinchu, Taiwan 300, Republic of China*

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The technology of polycrystalline silicon thin-film transistors (poly-Si TFTs) with low photoleakage current is developed in this work. The electrical characteristics of poly-Si TFTs under illumination were significantly improved employing the NH_3 plasma treatment on the buffer layer, with no need for complicate device structure and additional masks. The trap states that originated from the plasma bombardment on the interface between the poly-Si layer and buffer oxide can effectively recombine the light-induced electron-hole pairs. The fewer residual electron-hole pairs lead to the lower photoleakage current and improved subthreshold swing, as well as maintaining good electrical characteristics in the dark sate. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2912026]

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diode display.[1–3] The poly-Si TFTs offer great potential for active matrix display technology because of their superior electrical characteristics over those of amorphous silicon TFTs (*a*-Si TFTs). Recently, the demand of high-end mobile electronic products, such as digital camera, cell phone, and mobile TV, is continuing to rapidly grow, and so the high resolution and high image quality becomes the critical issue in the development of mobile displays. Therefore, the brightness of back light is getting higher and higher to meet the requirement for fine image quality and superior readability as people use these mobile electronic products under sunlight outdoors.[4,5] However, poly-Si TFTs usually suffer from undesirable photoleakage current under a high illumination environment.[6] The high leakage current and increased subthreshold swing (SS) of poly-Si TFT under illumination in AMLCDs should be reduced to avoid losing the charges stored in pixels. Therefore, the voltages that are held across the pixel electrodes would be diminished to affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. However, the researches about improving the electrical characteristics in poly-Si TFTs under illumination are very few and the mechanism of photoleakage current in poly-Si TFT is still not clarified.

In this work, without complicated device structure or process steps, a simple method to reduce the photoleakage current of poly-TFTs has been developed. The surface of buffer layer in the proposed poly-Si TFT is treated employing the NH_3 plasma to lower the photoleakage current and improve the SS characteristics under back-light illumination with the original characteristics of poly-Si TFTs

Top-gate *p*-type poly-Si TFTs with lightly doped drain (LDD) were fabricated in this letter. First of all, a 50-nm-thick SiN_x and a 150-nm-thick SiO_2 films were sequentially deposited to form buffer layer by plasma enhanced chemical vapor deposition (PECVD). Then, the surface of buffer layer was treated employing NH_3 plasma for 10 min. A thin 50-nm-thick undoped *a*-Si film was deposited by PECVD at 380 °C, followed by dehydrogenated via furnace annealing process at 450 °C. The *a*-Si films were crystallized by 308 nm XeCl excimer laser with the line-shaped beam power of 350 mJ/cm^2. The 100-nm-thick gate insulator was deposited by tetraethyl orthosilicate base oxide. The source/drain and LDD region were formed by the mass-separated ion implanter technique. The doping activation was performed by rapid thermal anneal irradiation. MoW was sputtered as a gate metal. The dimensions of TFTs in this work were the following: channel length (L) 6 μm, channel width (W) 6 μm, and the LDD length 1 μm.

Figure 1 shows the I_D-V_G transfer curves of conventional *p*-channel poly-Si TFT operated in linear region under the dark and photostates. The brightness of back light for photostate measurement is set as 3100 nit. As the gate bias is swept from 0 to 12 V, the leakage current of poly-Si TFTs in the dark state was about 10^{-13} A. With the same range of gate bias, the leakage current of poly-Si TFT under illumination is as high as two orders of magnitude, around 10^{-11} A. In addition, the SS is increased under illumination, about 0.45 V/decade, as the initial value in dark is 0.29 V/decade. The variation of SS is about 55%. The on/off current ratio of poly-Si TFTs was substantially reduced due to the high photoleakage current, so that the function of TFTs used as the pixel switch under illumination would be seriously affected.

Since the light emitted from the back light is mainly absorbed at the interface between the poly-Si layer and the

a)Electronic mail: tcchang@mail.phys.nsysu.edu.tw.

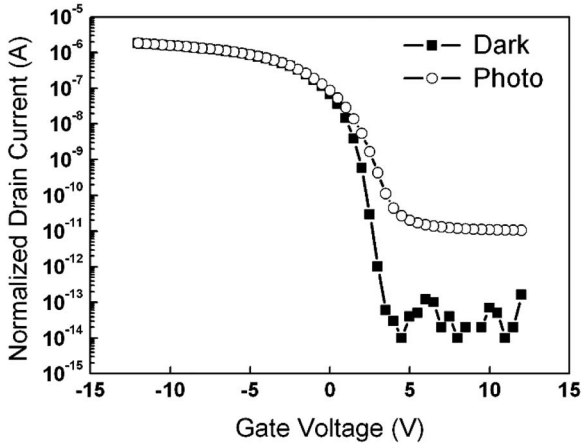


FIG. 1. I_D-V_G curves of the conventional poly-Si TFT operated in the linear region under illumination and dark states. A significantly increase of leakage current was found.

buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film.[7] Furthermore, the energy-band structure of Si material has indirect bandgap. The excess electron-hole pairs induced by the absorption of light would not be directly recombined from band to band due to the momentum conservation principle. The numerous electron-hole pairs are accumulated in the bottom of poly-Si layer. It follows that the excess holes flow to the drain under the negative drain bias for *p*-channel devices, generating the photoleakage current. To release the issue, the trap states on the surface of the buffer layer were induced by the NH_3 plasma treatment to assist the recombination of excess electron-hole pairs. Figure 2 plots the key process flow of proposed poly-Si TFTs. The surface quality in the top SiO_2 film of buffer layer would be degraded to generate the surface trap

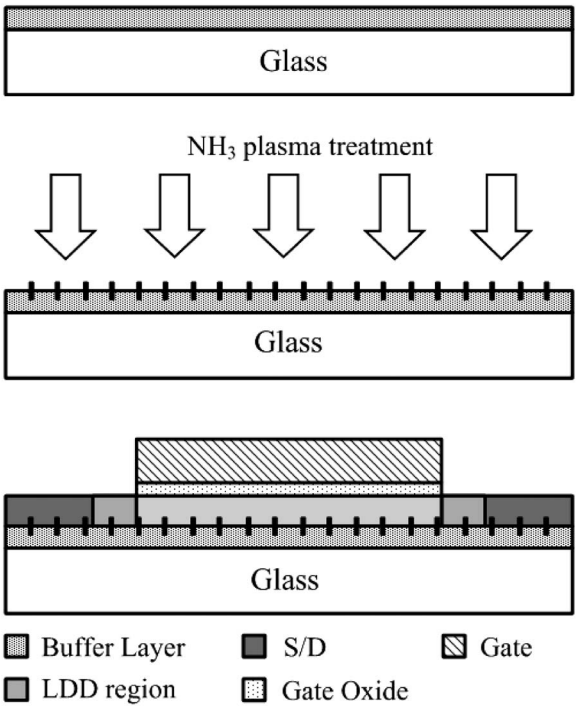
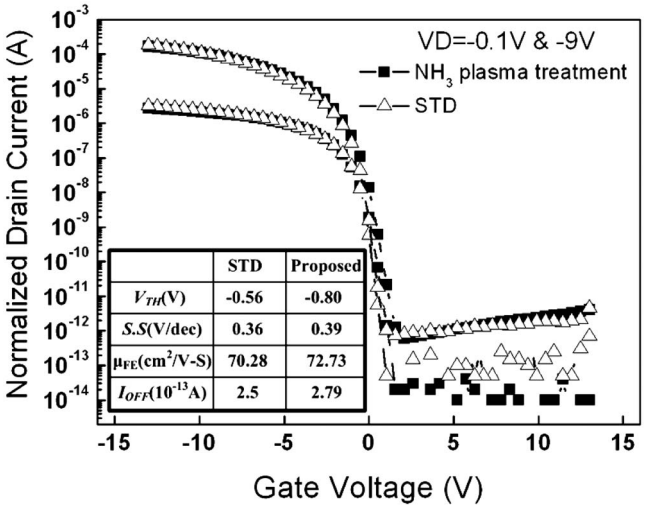


FIG. 2. The proposed process diagram for treating the surface of buffer layer using NH_3 plasma bombardment. Numerous state densities are generated to be taken as the recombination center for light-induced electron-hole pairs.



	STD	Proposed
V_{TH}(V)	-0.56	-0.80
S.S(V/dec)	0.36	0.39
μ_{FE}(cm^2/V-S)	70.28	72.73
I_{OFF}(10^{-13}A)	2.5	2.79

FIG. 3. The comparison of electrical characteristics in conventional and proposed TFT under dark state.

density employing the NH_3 plasma bombardment. After plasma treatment, the process flow is the same as the standard one.

Figure 3 shows the transfer curves of the conventional and proposed TFTs. The electrical characteristics of poly-Si TFTs with NH_3 plasma treatment on the buffer layer are almost entirely identical to the conventional ones. It is verified that the crystallization status of poly-Si would not be affected by the surface states of buffer layer. Therefore, the proposed method can be completely compatible with the conventional poly-Si process. Furthermore, in order to confirm the uniformity of poly-Si TFTs with proposed method, the average of key parameters extracted at linear operation in 12 TFTs with various location of substrate are summarized in the inset table of Fig. 3. It is found that the uniformity of proposed poly-Si TFTs kept in a good condition and the key parameters were nearly unchanged in comparison with the conventional devices.

The photoleakage current of the conventional and the proposed devices, which is extracted at a voltage $|V_G\text{-}V_t|$ of 7 V as V_D is 0.1 V, with the increasing brightness of back light (2160, 3100, 4110, and 5620 nit) are illustrated in Fig. 4(a). The photoleakage current of conventional poly-Si TFTs substantially increases with increasing brightness of back light. In contrast, for proposed device, the leakage current under illumination is slightly increased and there remains a weak dependence of the brightness of back light. The maximum of photoleakage current in the TFT with NH_3 plasma treatment is 8.1 pA. It is still much lower than 13.6 pA, the minimum of that in conventional TFT. Figure 4(b) shows the comparison of SS in the conventional and proposed TFTs under illumination with increasing brightness. The increasing ratio of SS, ΔSS, is defined as $(SS_{photo}/SS_{dark}-1)$, where SS_{photo} and SS_{dark} are the SS of devices at drain voltage of −0.1 V under photo and dark states. As the brightness of back light is 5610 nit, the maximum ΔSS of the conventional and proposed TFT are 46.4% and 85.3%, respectively. The significant improvement of variation in SS of poly-Si TFT under illumination is confirmed.

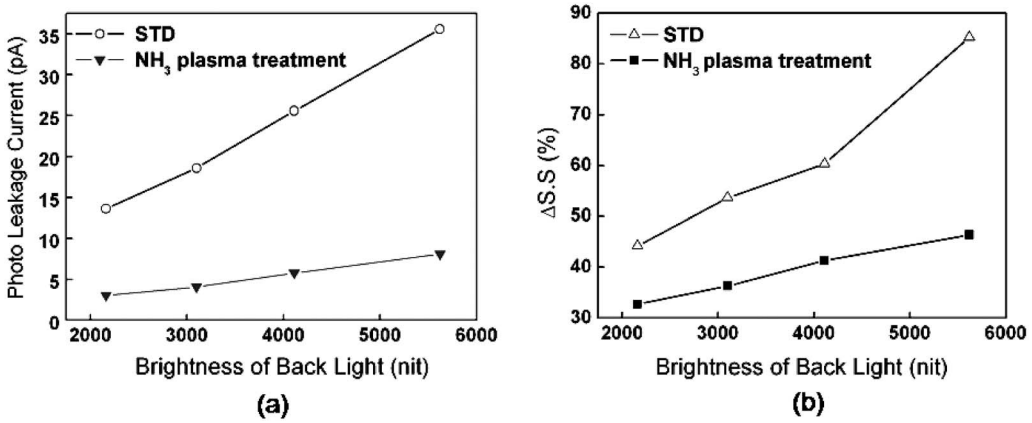


FIG. 4. As the brightness of back-light is set as 2160, 3100, 4110 and 5620 nit, (a)The comparison in photoleakage current of conventional and proposed devices; the remarkable reduction of photoleakage current in proposed TFT is observed. (b) the SS of conventional and proposed devices. As the brightness of back-light is 5610 nit, the maximum ΔSS of conventional and proposed TFT are 46.4% and 85.3%

In conclusion, we have demonstrated a simple method to fabricate the poly-Si TFT with low photoleakage current without changing the structure or process flow. The proposed poly-Si TFT exhibits the impressively low leakage current and improved SS under illumination. The uniformity and electrical characteristics of proposed devices are almost same as the conventional ones. As the brightness of back light is set to 5610 nit, the photoleakage and the variation of SS in proposed TFT are 8.1 pA and 46.3%, respectively while those in conventional TFT are 35.6 pA and 85.3%.

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