Electrical Properties of Low-Temperature-Compatible P-Channel Polycrystalline-Silicon TFTs Using High-κ Gate Dielectrics

Ming-Jui Yang, Chao-Hsin Chien, *Associate Member, IEEE*, Yi-Hsien Lu, Chih-Yen Shen, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—In this paper, we describe a systematic study of the electrical properties of low-temperature-compatible p-channel polycrystalline-silicon thin-film transistors (poly-Si TFTs) using HfO_2 and $HfSiO_x$ high-κ gate dielectrics. Because of their larger gate capacitance density, the TFTs containing the high-κ gate dielectrics exhibited superior device performance in terms of higher I_{on}/I_{off} current ratios, lower subthreshold swings (SSs), and lower threshold voltages (V_{th}), relative to conventional deposited-SiO_2, albeit with slightly higher OFF-state currents. The TFTs incorporating $HfSiO_x$ as the gate dielectric had ca. 1.73 times the mobility (μ_{FE}) relative to that of the deposited-SiO_2 TFTs; in contrast, the HfO_2 TFTs exhibited inferior mobility. We investigated the mechanism for the mobility degradation in these HfO_2 TFTs. The immunity of the $HfSiO_x$ TFTs was better than that of the HfO_2 TFTs—in terms of their V_{th} shift, SS degradation, μ_{FE} degradation, and drive current deterioration—against negative bias temperature instability stressing. Thus, we believe that $HfSiO_x$, rather than HfO_2, is a potential candidate for use as a gate-dielectric material in future high-performance poly-Si TFTs.**

***Index Terms*—Hafnium silicate ($HfSiO_x$), high dielectric constant (high-κ), negative bias temperature instability (NBTI), polycrystalline-silicon thin-film transistors (poly-Si TFTs).**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si TFTs) are employed extensively in active-matrix liquid crystal displays because of their superior performance [1]. Recently, the practicability of integrating the entire system on the panel has been investigated vigorously [2]. This goal requires that the display driving circuits contain high-performance TFTs capable of operating at lower voltages while delivering higher drive currents. Although scaling down the gate oxide can increase the drive current of a TFT, it leads inevitably to a higher gate leakage current because of the decreased quality of the low-temperature-deposited gate dielectrics [3]. To maintain the physical dielectric thickness while increasing the gate capacitance, several new high-κ materials have been proposed, including Al_2O_3, Ta_2O_5, and HfO_2 [4]–[6]. Because Al_2O_3 films exhibit relatively low values of κ (ca. 7) and excess fixed charge, the TFT performance is not improved sufficiently for application [7]. The narrow band-gap of Ta_2O_5 means that a thicker film is necessary to reduce the gate leakage current of TFTs [8], which limits the increase in gate capacitance. Recently, hafnium dioxide (HfO_2) has been applied to TFTs because of its high value of κ (14 to 20) and sufficiently wide band-gap [6]. Although poly-Si TFTs incorporating HfO_2 as the gate dielectric exhibit superior performance in many respects, several issues remain problematic, e.g., the higher gate leakage current arising from polycrystalline HfO_2 films and the degraded mobility arising from additional scattering. In this paper, we employed HfO_2 and $HfSiO_x$ as gate dielectrics for p-channel poly-Si TFTs and found that the transistors containing high-κ dielectrics exhibited higher values of I_{on}/I_{off} and μ_{FE} and smaller values of subthreshold swing (SS) and V_{th}, relative to transistors containing a conventional deposited-SiO_2 dielectric. We also studied the instability of these TFTs under negative bias temperature instability (NBTI) stress. By measuring and analyzing the transfer characteristics before and after stressing for various stress times and temperatures, we determined the effects of NBTI on the poly-Si TFTs incorporating high-κ dielectrics.

Manuscript received September 21, 2007; revised December 26, 2007. This work was supported in part by the National Science Council, Taiwan, R.O.C., under Contract 95-2221-E-009-313. The review of this paper was arranged by Editor M. J. Kumar.

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Digital Object Identifier 10.1109/TED.2008.916759

II. Device Fabrication

Self-aligned top-gated p-channel poly-Si TFTs were fabricated. First, a 550-nm-thick thermal oxide was grown on Si wafers in a furnace to simulate the glass substrate. Next, a 100-nm-thick amorphous-silicon layer was deposited through the dissociation of SiH_4 gas in a low-pressure chemical-vapor-deposition (LPCVD) system at 550 °C. Subsequently, solid-phase crystallization was performed at 600 °C for 24 h in N_2

ambient to induce the crystallization of amorphous silicon. Individual active regions were then patterned by lithography and defined by dry etching. After cleaning, various gate dielectrics (each 60-nm thick) were deposited. Specifically, HfO_2 and $HfSiO_x$ films were deposited through atomic-vapor deposition using an AIXTRON Tricent System at a substrate temperature of 500 °C. The $Hf[OC(CH_3)_3]_2(mmp)_2$ precursor, $Si(mmp)_4$ precursor, and oxygen gas were employed as Hf, Si, and O sources, respectively. The as-deposited oxide, which served as the control sample, was prepared through LPCVD at 700 °C using tetraethyloxysilane as the precursor. All of the wafers were then subjected to deposition of a 300-nm-thick amorphous-silicon layer, which served as the gate electrode, through LPCVD at 550 °C. The gate electrodes were patterned, and the source, drain, and gate regions were doped through self-aligned boron ion implantation (dosage: 5×10^{15} ions/cm^2; energy: 15 keV). After the formation of the source and drain, the dopant was activated at 600 °C for 24 h in N_2 ambient. Following that, 500-nm SiO_2 was deposited by plasma-enhanced CVD as the interlayer dielectric. Finally, contact holes were opened, and 550-nm AiSiCu alloy was deposited and defined. The wafers were then sintered at 400 °C for 30 min in forming gas to complete the fabrication. Capacitors containing high-κ dielectrics were fabricated simultaneously through the use of a shadow mask to allow measurement of dielectric constants and leakage current densities. Device measurements were performed using a Keithley 4200 semiconductor characterization system, an HP 4156A precision semiconductor parameter analyzer, and an Agilent 4284A precision LCR meter. The field-effect mobility, which was extracted from the maximum transconductance (G_m), and the SS were measured at a value of V_{DS} of -0.1 V. The value of the SS was extracted from the maximum slope of the $I_{DS}-V_{GS}$ characteristics. The threshold voltage was defined as the gate voltage at which the drain–current reached a normalized drain–current (I_D) equal to $(W/L) \times 10^{-8}$ A at a value of V_{DS} of -0.1 V, where W is the drawn channel width and L is the drawn channel length. During NBTI stressing, the substrate was heated to the stress temperature (ranging from 25 °C to 100 °C), and then, the stress bias of 2 MV/cm was applied to the gate with the source and drain grounded. The stress was removed periodically to measure the basic device characteristics and to characterize the NBTI effect; all measurements were performed at the stress temperature.

III. Results and Discussion

Fig. 1 shows cross-sectional transmission-electron-microscopy (TEM) images of the HfO_2, $HfSiO_x$, and deposited-SiO_2 films, which had physical thicknesses of 57, 53, and 61 nm, respectively. The $HfSiO_x$ and deposited-SiO_2 films both possessed amorphous structures, which were conducive to forming smoother surfaces at both the top and bottom interfaces, whereas the HfO_2 film revealed a polycrystalline structure. Atomic-force microscopy revealed similar features (data not shown). The mean surface roughnesses of the $HfSiO_x$ and deposited-SiO_2 films were 0.42 and 0.60 nm, respectively—much smaller than that (1.97 nm) of the HfO_2 film. For further analysis, we used X-ray diffraction

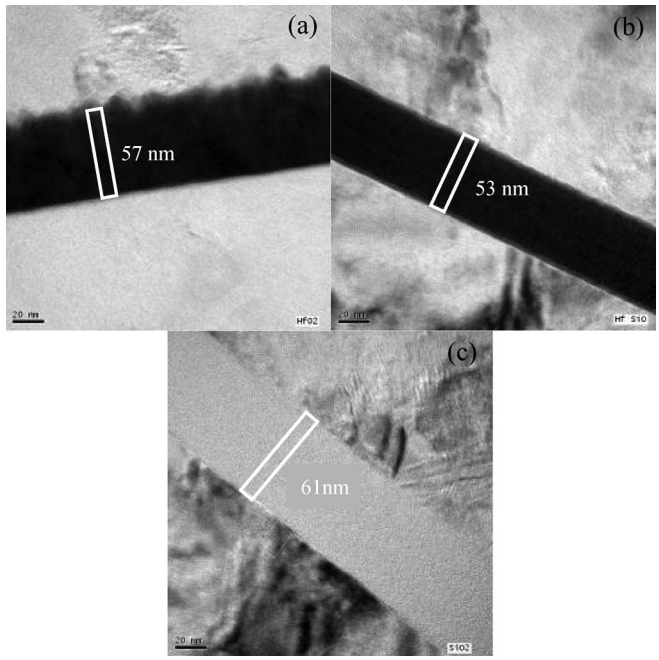

Fig. 1. Cross-sectional TEM images of TFTs incorporating (a) HfO_2, (b) $HfSiO_x$, and (c) deposited-SiO_2 gate dielectrics.

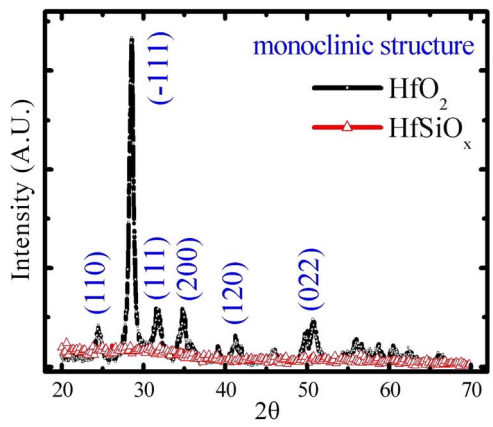

Fig. 2. X-ray diffraction patterns of HfO_2 and $HfSiO_x$ films after annealing for 24 h at 600 °C in a N_2 ambient.

spectroscopy (XRD) to investigate the crystallinity of the HfO_2 and $HfSiO_x$ films (Fig. 2). After annealing at 600 °C and 24 h in a N_2 ambient, the HfO_2 film clearly exhibited a polycrystalline monoclinic structure, whereas the $HfSiO_x$ film retained its amorphous form. This behavior suggests that the $HfSiO_x$ film had better thermal stability than did the HfO_2 film.

Fig. 3(a) and (b) provide plots of the capacitance density versus the gate voltage and the leakage-current density versus the electrical field, respectively, for the high-κ dielectrics. The extracted value of κ for the HfO_2 film was ca. 14.2, which is significantly lower than that of bulk HfO_2, possibly because of the following reasons: 1) the presence of excess oxygen atoms in the HfO_2 film [9] and 2) the fact that the mode effective charges associated with the softest modes are relatively weak when the HfO_2 film possesses its most stable monoclinic structure [10], [11]. On the other hand, the value of κ for the $HfSiO_x$ film was

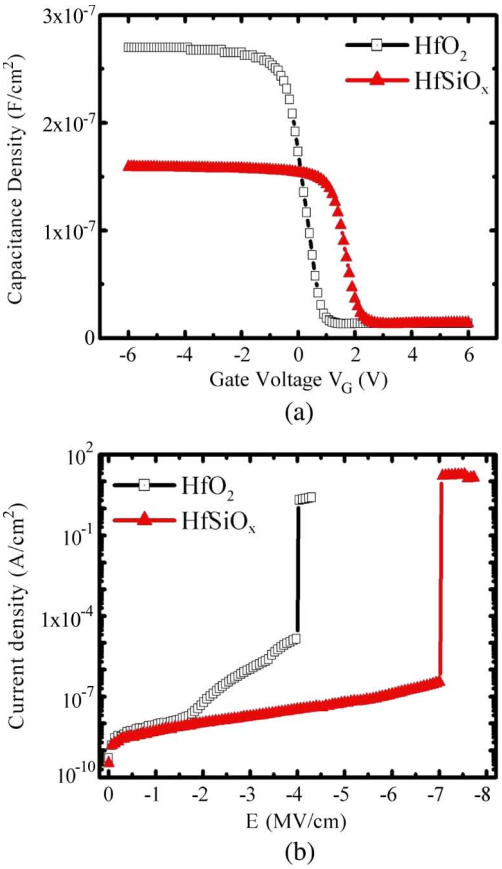

Fig. 3. Plots of (a) capacitance density versus gate voltage and (b) leakage-current density versus electrical field for the HfO_2 and $HfSiO_x$ films obtained after annealing for 24 h at 600 °C in a N_2 ambient.

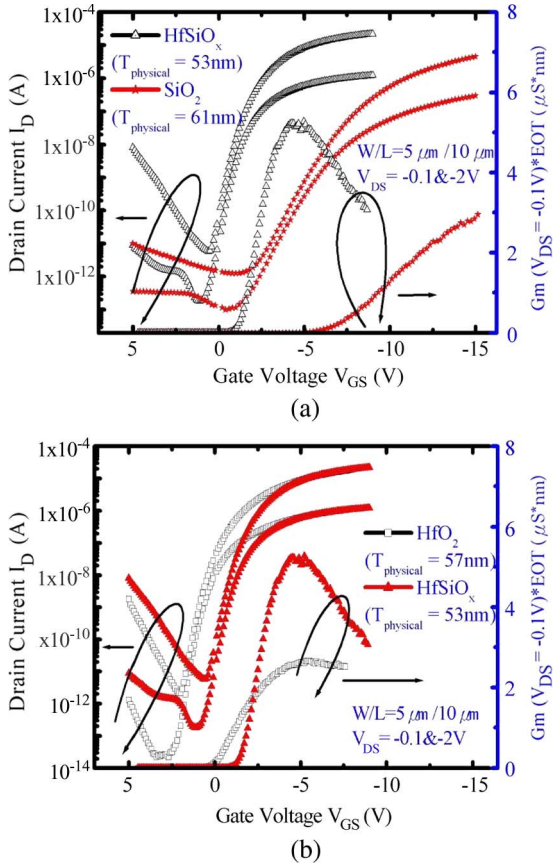

Fig. 4. Comparisons of the transfer characteristics at values of V_{DS} of -0.1 and -2 V between the TFTs containing (a) $HfSiO_x$ and deposited-SiO_2 and (b) $HfSiO_x$ and HfO_2 as gate dielectrics.

ca. 8.11, which is also lower than expected. The Hf/Si composition ratio (ca. 1 : 1.44) calculated from this value of κ was close to that (1 : 1.38) measured using electron spectroscopy for chemical analysis (ESCA; data not shown). This result indicates that Si atoms are more reactive toward oxygen atoms than are Hf atoms under our process conditions; therefore, the lower dielectric constant of the $HfSiO_x$ films is due to their being Si-rich. In terms of the films' current–voltage characteristics, the $HfSiO_x$ film exhibited superior performance—a smaller leakage current (7.60×10^{-8} A/cm^2 at $V_{GS} = -10$ V) and a larger breakdown field (-7 MV/cm)—relative to that of the HfO_2 film (4.70×10^{-9} A/cm^2 and -4 MV/cm, respectively), presumably because of the amorphous nature of $HfSiO_x$ after processing. Fig. 4(a) and (b) provide comparisons of the transfer characteristics between the TFTs containing $HfSiO_x$ and deposited-SiO_2 and between the TFTs containing $HfSiO_x$ and HfO_2, respectively, at values of V_{DS} of -0.1 and -2 V. Table I summarizes the measured data and the extracted device parameters. The TFTs containing the high-κ dielectrics displayed considerably better performance than did the TFT containing the conventional deposited-SiO_2, with the exception of their OFF-state leakage currents. In addition to the superior quality of the gate-dielectric–poly-Si interface [5], we believe that the thinner equivalent oxide thicknesses of the high-κ dielectrics at the same physical thickness accounts for the lower value of V_{th} and the significantly improved SS [12], [13]. Moreover, we have reported previously that the values of V_{th} and SS are sensitive to the density of deep states near the midgap; i.e., as the densities-of-state decreases, the values of V_{th} and SS decrease [14]. This behavior is supported by the plots of the density-of-state versus ΔE (where $\Delta E = E - E_{FB}$) for the poly-Si TFTs incorporating the various gate dielectrics (Fig. 5). The values of densities-of-state were extracted from the transfer characteristics measured at 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C [15]. We found that the high-κ dielectrics did possess lower densities-of-state. On the other hand, the effective interface-trap-state density (N_{it}) near the poly-Si–gate-dielectric interface can be evaluated from the value of SS [16]

$$N_{it} = \left[\left(\frac{S}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{\text{gate dielectric}}}{q}\right). \quad (1)$$

The calculated values of N_{it} for the HfO_2, $HfSiO_x$, and deposited-SiO_2 TFTs were 5.60×10^{12}, 4.44×10^{12}, and 7.86×10^{12}/cm^2, respectively. Thus, this approach also reveals that the high-κ dielectrics possess lower densities-of-state relative to that of the deposited-SiO_2.

Although the values of the SS and I_{on}/I_{off} current ratio of the TFTs containing $HfSiO_x$ were slightly worse than those of the TFTs incorporating HfO_2, we believe that $HfSiO_x$ is the better choice for use as the gate dielectric in future poly-Si TFTs for the following reasons. First, the TFTs containing $HfSiO_x$ films exhibited the smaller leakage-current densities

TABLE I
DEVICE PARAMETERS OF LOW-TEMPERATURE P-CHANNEL POLY-Si TFTS ($W/L = 5\ \mu m/10\ \mu m$) INCORPORATING VARIOUS GATE DIELECTRICS AT A VALUE OF V_{DS} OF -0.1 V

Gate dielectric	I_{on}/I_{off} ratio (@V_{DS}= -2V)	S. S. (V/Dec)	V_{th} (V)	μ_{FE} (cm^2/V-sec)	EOT (nm)
HfO_2 ($T_{physical}$= 57nm)	8.95E6 (V_{GS}= -8V)	0.30	0.25	15.37	15.7
$HfSiO_x$ ($T_{physical}$= 53nm)	3.79E6 (V_{GS}= -8V)	0.37	-1.13	30.41	25.5
Deposited-SiO_2 ($T_{physical}$= 61nm)	3.65E6 (V_{GS}= -15V)	1.06	-6.90	17.61	46.5

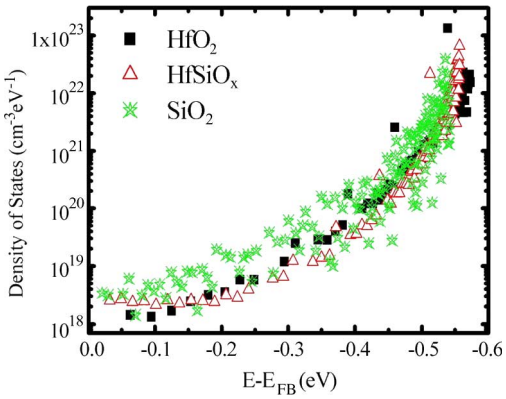

Fig. 5. Densities-of-state extracted from the transfer characteristics ($V_{DS} = -0.1$ V) of poly-Si TFTs incorporating various gate dielectrics.

TABLE II
ETCHING RATES OF VARIOUS GATE DIELECTRICS

Gate dielectric	BOE etching	ICP dry etcher	
		CF_4/CHF_3	Cl_2
HfO_2	0 nm/sec	0.4 nm/sec	1.3 nm/sec
$HfSiO_x$	0.65 nm/sec	1.1 nm/sec	2.6 nm/sec
Deposited-SiO_2	10 nm/sec	6.5 nm/sec	3.5 nm/sec

and larger breakdown fields than did the HfO_2 TFTs because of the amorphous nature of the $HfSiO_x$ film after processing. Second, the hole mobility of the TFTs containing $HfSiO_x$ was 73% better than that of the conventional TFTs incorporating the deposited-SiO_2 dielectric, whereas it was worse for the TFTs containing HfO_2. According to previous reports [17]–[19], we speculate that the degraded mobility of the TFTs containing the HfO_2 dielectric is due to additional Coulomb scattering caused by the charges in the HfO_2 dielectric. In conventional MOSFETs, additional Coulomb scattering is closely related to the polycrystalline structure of the HfO_2 films, which in turn leads to severe mobility degradation in devices possessing physically thicker HfO_2 films [18]. In contrast, $HfSiO_x$ films prevent this additional scattering and exhibit improved mobility because of their higher thermal stability. Third, the removal of $HfSiO_x$ through etching is much easier than that of HfO_2. This feature is rather important for device fabrication. We employed a buffer-oxide-etch (BOE) solution and an induced-coupling-plasma (ICP) etcher to perform wet and dry etching, respectively. Table II summarizes the etching rates for the various dielectrics when using the two etching methods and various gases. The HfO_2 film could not be etched away; its thickness remained nearly constant after wet etching for 1 min. For dry etching, we found that the etching rate for HfO_2 film with CF_4/CHF_3 mixing gas (0.4 nm/s) was much lower than that for the deposited SiO_2 (6.5 nm/s). Even though the etching rate could be increased to 1.3 nm/s when using Cl_2 gas, the poly-Si channel was more vulnerable to etching damage because of its relatively high etching rate of 3 nm/s. In contrast, the $HfSiO_x$ films could be removed by the BOE solution at a rate of 0.65 nm/s, and the dry etching rates were also faster than those of the HfO_2 films. As a result, less etching damage occurs at the $HfSiO_x$-film–poly-Si interface of contact regions when using a sequence of dry etching followed by wet etching near the end of the etching process.

Although the TFTs incorporating the high-κ gate dielectrics exhibited better ON-state electrical properties than did the conventional TFT containing deposited-SiO_2, much more severe effects of gate-induced drain leakage (GIDL) were clearly evident in the plots of the transfer characteristics of the high-κ TFTs. To further clarify the mechanism of the larger OFF-state current, the activation energies of the different gate dielectrics were calculated from the I_{DS}–V_{GS} curves obtained at 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C. Fig. 6(a) and (b) present plots of the dependence of activation energy (E_a) on V_{GS} at values of V_{DS} of -0.1 and -2 V, respectively. At the lower value of V_{DS}, the TFT containing HfO_2 had the highest activation energy accounting for the depicted lowest minimum leakage current. Upon increasing $|V_{GS}|$ in the OFF-state regime, the activation energy of the TFT incorporating HfO_2 decreased drastically, whereas those containing $HfSiO_x$ and deposited SiO_2 exhibited smooth decreases in their activation energies. When the value of V_{DS} was -2 V, all of the TFTs exhibited rapidly decreasing values of E_a upon increasing $|V_{GS}|$. To explain these results, we must consider the leakage mechanisms of the poly-Si TFTs in the OFF-state [20]–[24]. Typically, the OFF-state current in the poly-Si TFTs can be divided into the following three parts: 1) in the region of very low $|V_{GS}|$, the increasing OFF-state current as $|V_{GS}|$ increases is related to the resistive current, which is assumed to be an ohmic current flowing through the poly-silicon layer; 2) in the almost-flat region, the OFF-state current that does not change with increasing $|V_{GS}|$ is related to the thermal-generation current, which was reported to be nearly independent of $|V_{GS}|$ [20]; and 3) in the high-$|V_{GS}|$ region, the increasing OFF-state current as $|V_{GS}|$ increases is linked to the thermionic field or Frenkel–Poole emission current, which is due to field-enhanced thermal excitation. In Fig. 4, we observe

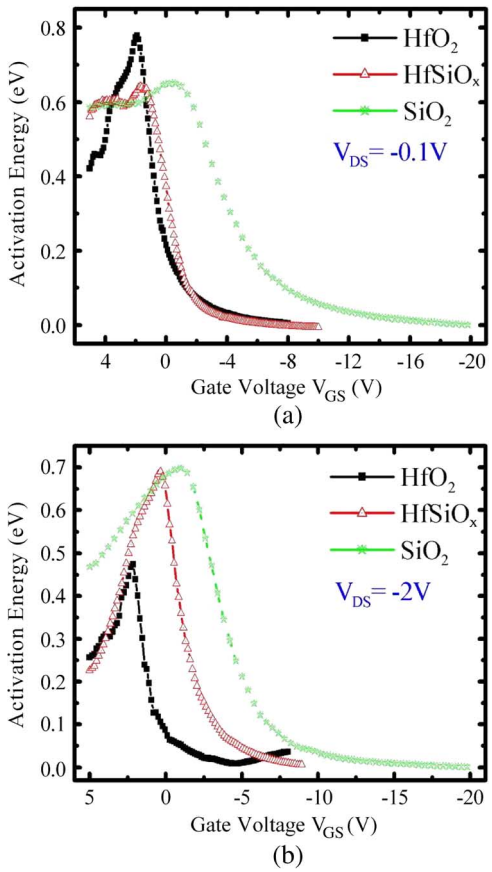

Fig. 6. Channel activation energies obtained from the temperature dependence of the transfer characteristics of the poly-Si TFTs incorporating various gate dielectrics at values of V_{DS} of (a) -0.1 and (b) -2 V.

clearly that the OFF-state current was dominated by the resistive current and thermal-generation current for the TFTs containing deposited-SiO_2 gate dielectrics at a value of V_{DS} of -0.1 V. When V_{DS} was increased to -2 V, the thermal-generation current prevailed in the low-$|V_{GS}|$ regime, and the Frenkel–Poole emission current preponderated in the high-$|V_{GS}|$ regime. On the other hand, we found that the OFF-state currents in the $HfSiO_x$ TFTs at a value of V_{DS} of -0.1 V were resistive, thermal generation, and Frenkel–Poole emission currents in the low-, intermediate-, and high-$|V_{GS}|$ ranges, respectively; in contrast, only the Frenkel–Poole emission current was present when V_{DS} was -2 V for the all of the $|V_{GS}|$ ranges. The HfO_2 TFTs exhibited similar behavior, although the Frenkel–Poole emission current prevailed over the other two currents, even when V_{DS} was -0.1 V. We speculate that these results are closely related to the higher values of κ possessed by the high-κ dielectrics. According to the Frenkel–Poole emission mechanism, the OFF-state current is highly dependent on the peak electric field (E_{pk}) at the drain junction and is dominated by the vertical electric field at the interface; thus

$$I_{FE} \propto \exp(\sqrt{E_{pk}}$$
$$E_{pk} = \frac{(V_{GS} - V_{DS} - V_{FB})\varepsilon_{\text{gate dielectric}}}{(T_{\text{gate dielectric}}\varepsilon_{Si})} \quad (2)$$

where ε_{Si} and $\varepsilon_{\text{gate dielectric}}$ are the permittivities of Si and the gate dielectric, respectively, V_{FB} is the flatband voltage defined as minimum I_{DS}, and $T_{\text{gate dielectric}}$ is the physical thickness of the gate dielectric. The poly-Si TFTs incorporating the high-κ gate dielectrics definitely exhibited their higher peak electric fields as a result of their higher values of κ (because the physical thicknesses of all the dielectrics were similar), which then caused the rapidly increasing Frenkel–Poole emission currents. These results can also be explained by considering the plots of the activation energy. At a low drain-to-gate bias $|V_{DG}|$, the thermal-generation current was the dominant leakage-current mechanism, and the corresponding value of E_a was higher. As $|V_{DG}|$ increased, the Frenkel–Poole emission current gradually became the preeminent leakage mechanism, and the value of E_a, which was most significant to the thermal-generation current, decreased rapidly. As a result, we suggest that lightly doped drain, multigate, and offset structures, which can reduce the electrical field between the drain and the channel of the TFT, could be applied to suppress the deterioration of the OFF-state current when high-κ dielectrics are employed as gate dielectrics.

We also studied the instability of the low-temperature p-channel poly-Si TFTs possessing the various gate dielectrics under NBTI stress. Fig. 7(a)–(d) display the variations in the values of V_{th}, SS, μ_{FE}, and the drive current as functions of the NBTI-stress time. Initially, the deposited-SiO_2 TFT displayed less of a shift in V_{th} and the drive-current degradation than did the other two TFTs. In contrast, the TFTs incorporating the high-κ dielectrics exhibited less degradation than did those containing deposited SiO_2 for all of these parameters when the stress period increased; specifically, the $HfSiO_x$ TFT exhibited the strongest immunity against stress. We believe that these results are closely related to the fact that the trapped charge accumulates in the high-κ dielectric via filling, rather than through generation, which occurs in the deposited-SiO_2 [25], [26]. According to previous reports [27]–[30], we attribute the degradation of both SS and μ_{FE} mainly to interface-trap-state generation. The NBTI stress, which causes bonds to break at the poly-Si–gate dielectric interface and generates more dangling bonds, results in the increased number of interface trap states. Our results proved that the $HfSiO_x$ film possessed the superior interface quality; i.e., fewer traps would be created during the application of stress. Based on formula (1), we estimated the N_{it} increment to be only 6.43% for the $HfSiO_x$ TFT after stressing. This value was much lower than those for the TFTs containing the HfO_2 and deposited-SiO_2 films (both ca. 19%). In addition, the V_{th} shift in the poly-Si TFTs caused by the NBTI stress is also governed by the generation of grain-boundary traps in the channel [30]. To investigate the effects of the grain-boundary traps during NBTI stress, we used the Levinson–Proano method to estimate the grain-boundary trap densities (N_{trap}) for all of the samples [31], [32]. Fig. 8(a)–(c) present the plots of $\ln[I_{DS}/(V_{GS} - V_{FB})]$ versus $1/(V_{GS} - V_{FB})^2$ at a value of V_{DS} of -0.1 V and at high V_{GS}, where the flatband voltage (V_{FB}) is defined as the gate voltage that yields the minimum drain current from the transfer characteristic. We found that the $HfSiO_x$ TFT not only provided the lowest initial value of N_{trap} but also the highest immunity

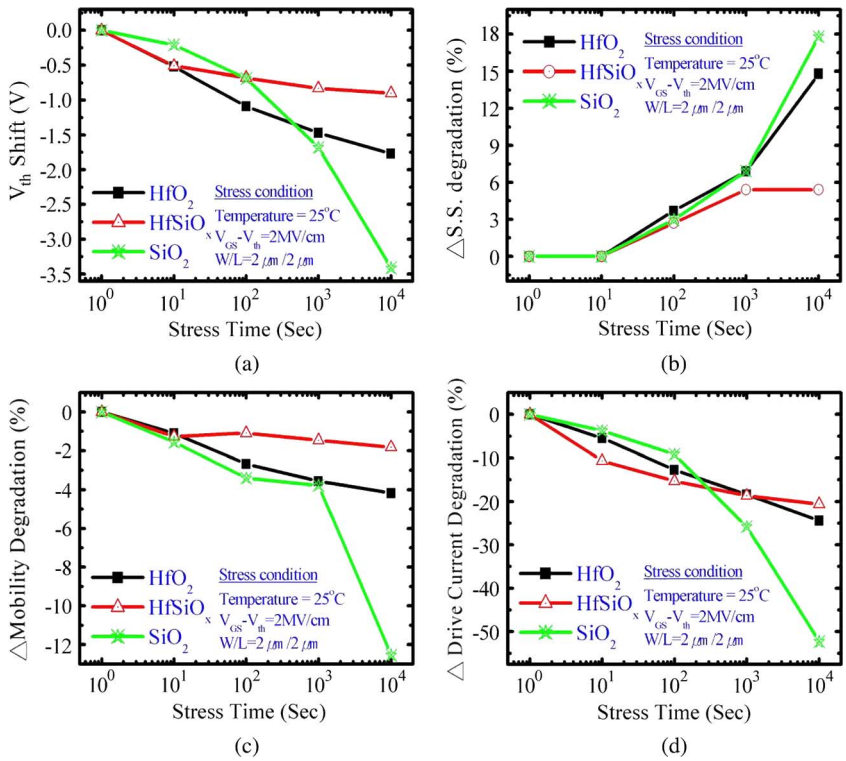

Fig. 7. Values of (a) $V_{\rm th}$, (b) SS, (c) $\mu_{\rm FE}$, and (d) the drive current of the poly-Si TFTs incorporating various gate dielectrics, plotted with respect to the stress time at 25 °C.

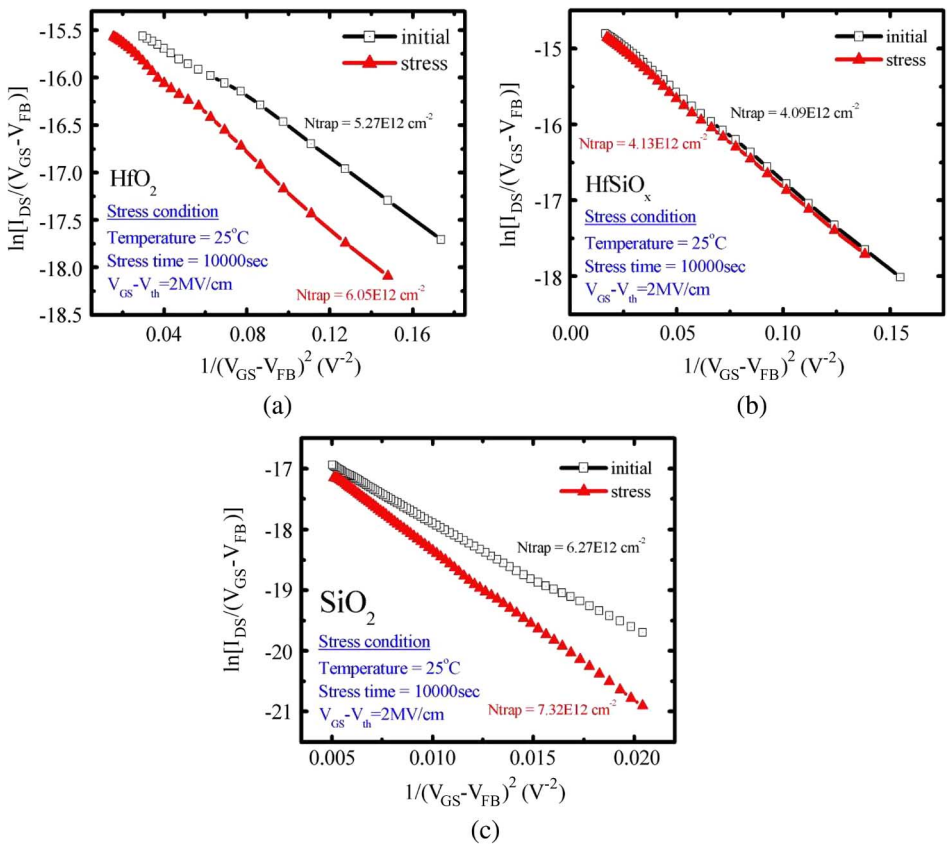

Fig. 8. Grain-boundary trap-state density extraction of the poly-Si TFTs incorporating (a) HfO_2, (b) $HfSiO_x$, and (c) deposited-SiO_2 gate dielectrics before and after NBTI stressing for 10 000 s at 25 °C; stress bias: $V_{\rm GS} - V_{\rm th} = 2$ MV/cm.

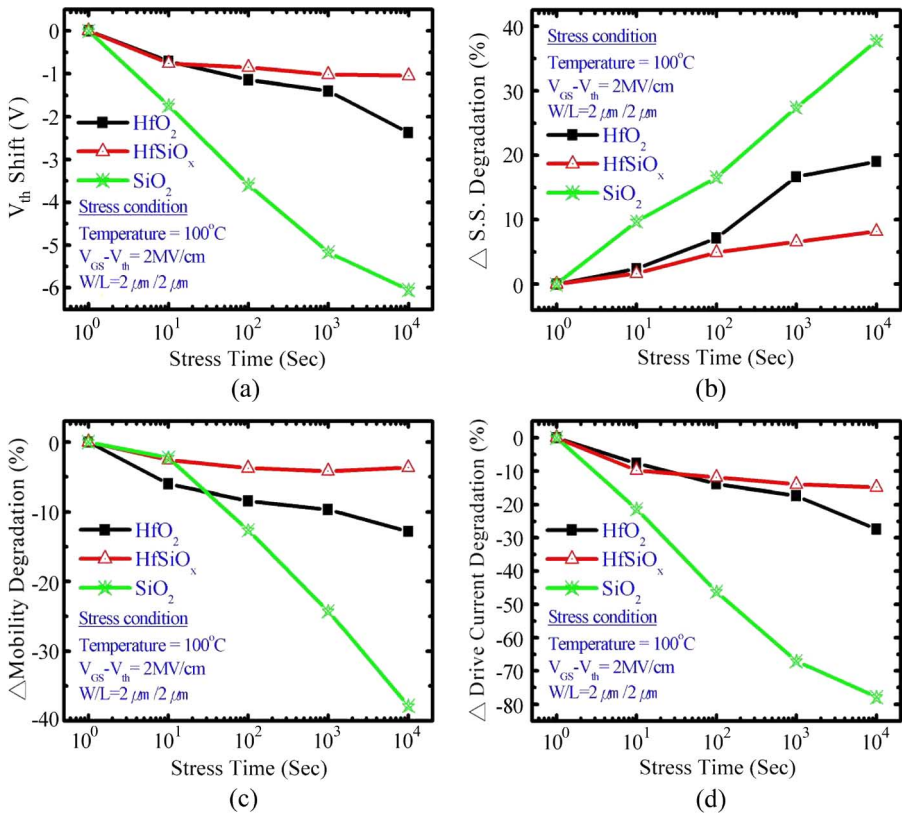

Fig. 9. Values of (a) $V_{\rm th}$, (b) SS, (c) $\mu_{\rm FE}$, and (d) drive current of the poly-Si TFTs incorporating various gate dielectrics, plotted with respect to the stress time at 100 °C.

against $N_{\rm trap}$ creation during stressing, although the detailed mechanism is not clear at present. As a consequence, we expect less degradation of the drive currents of $HfSiO_x$ TFTs, because the drive-current degradation is mainly attributed to the $V_{\rm th}$ shift and the decrease in $\mu_{\rm FE}$. Fig. 9(a) and (b) display the variations of $V_{\rm th}$, SS, $\mu_{\rm FE}$, and the drive current as a function of the NBTI-stress time at 100 °C. Although the tendencies are similar to those revealed at room temperature, we note that the TFTs containing the high-κ dielectrics were relatively insensitive to high temperature, whereas the deterioration of the deposited-SiO_2 TFT was dramatic. This feature seems very favorable for TFTs to be fabricated on displays, because glass substrates have very poor thermal conductivity. As a result, using high-κ gate dielectrics cannot only enhance the performance of poly-Si TFTs but also improve their reliability over those incorporating conventional deposited-SiO_2. In addition, $HfSiO_x$ appears to have better potential over HfO_2 for use as a future gate dielectric in low-temperature-compatible poly-Si TFTs.

IV. Conclusion

In this paper, we have demonstrated that low-temperature p-channel poly-Si TFTs incorporating high-κ gate dielectrics exhibit improved performance and long-term stability—i.e., higher values of $\mu_{\rm FE}$ and $I_{\rm on}/I_{\rm off}$, smaller values of SS and $V_{\rm th}$, and superior NBTI reliability—relative to TFTs containing conventional deposited-SiO_2. Our results suggest that $HfSiO_x$ is a more suitable candidate than HfO_2 for use as a gate-dielectric material in future high-performance poly-Si TFTs.

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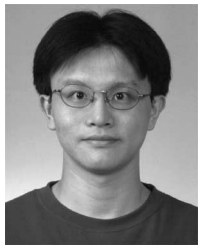

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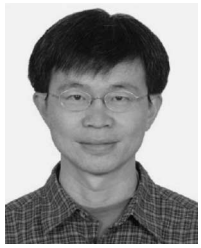

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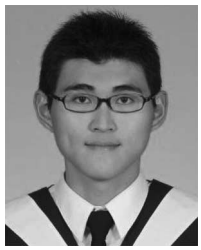

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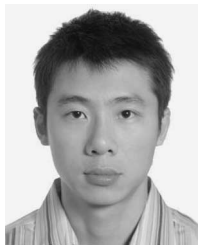

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