對稱式現場可程式閘陣列導線段結構之設計和可繞度之分析

Design and Analysis of Symmetric Array-Based FPGA Segmentations

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一、英文摘要

Logic circuits are implemented in an FPGA by partitioning logic into logic modules and then interconnecting the modules. FPGA interconnection resources consist of pre-fabricated wire segments and programmable switches. Routing in FPGA is performed by programming the switches to connect the wire segments. Recent work has shown that the feasibility of FPGA design is constrained more by routing resources than by logic resources, and often routing delays, rather than logic-module delays, dominate the performance of FPGAs. Therefore, it is of significant importance to consider the routing architectures for FPGA design.

For the two major types of FPGAs, row-based and symmetric array-based FPGAs, the symmetric array-based ones are the most popular architecture. Unlike switch modules and row-based segmentations which have been intensively studied, not much work was reported on the design of symmetric array-based segmentations (partly because of its high design complexity).

In this project, we shall explore the segmentation design problem for symmetric array-based FPGAs. There are three competing considerations in the design of FPGA routing architecture: routability, area, and speed. Hence, the objective of the problem is designing wire segments in the interconnection channels to maximize net routability and satisfy area and timing requirements simultaneously. We propose to study the problem from a wide spectrum of approaches based on the combinatorial, analytical, and stochastic models and extensive experiments as well. Architecture and computer-aided design (CAD) are two closely related issues (e.g., routing architectures and routers); the quality of a segmentation design needs to be evaluated by a router, and it is desirable for a router to consider segmentation architectures. Thus, the study shall significantly contribute not only to the architectural decisions, but also to the router design for the symmetric array-based FPGAs.

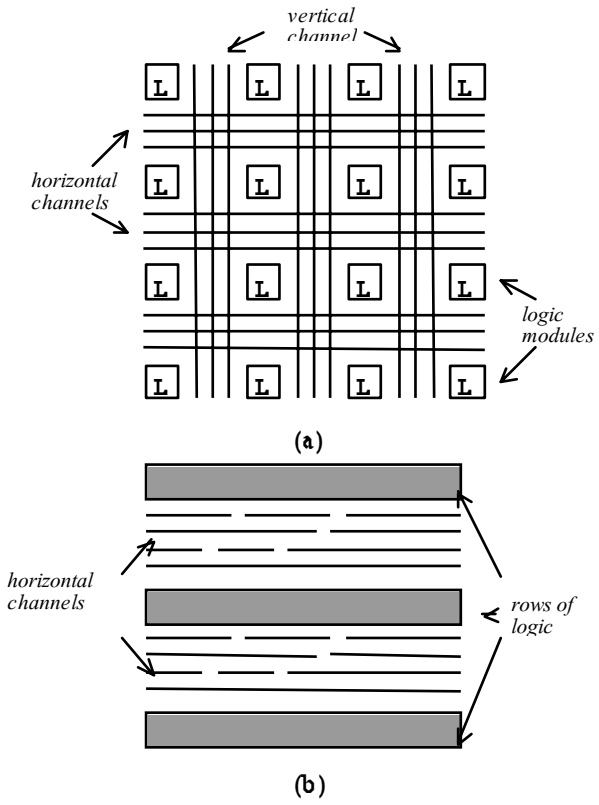
文摘要

使用現場可程式化閘陣列（FPGA）製作邏輯電路，首先須切分邏輯以便每個子電路皆能置入相關的邏輯模組中，然後在於各邏輯模組間作線路的連接。FPGA 的繞線資源包含導線段及可程式化開關；其繞線爲藉由控制開關以完成導線段的連通。近年的研究顯示：FPGA 設計的可行性最主要受限於繞線資源（而非邏輯資源）；而 FPGA 的效能最主要取決於繞線的速度（而非邏輯閘的速度）。因此繞線的結構實爲 FPGA 設計最關鍵的部分。

目前 FPGA 有兩種最主要的類型：橫列型及對稱陣列型(見圖一)，而以對稱陣列型最受歡迎。然而相較於對開關模組及橫列型導線段的大量研究，目前對於對稱陣列型 FPGA 繞線結構的探討卻顯不足（部分原因乃由於對稱陣列型 FPGA 結構的高複雜度對其研究所造成之困擾）。

本計畫的目的在於建立一套有系統的方法，希望對於對稱陣列型 FPGA 的導線段結構的設計與分析有所突破。FPGA 的繞線結構設計有三項相互競爭的考量：可繞度、面積及速度。而導線段結構設計的基本目標在於設計出能夠同時滿足面積及速度要求下，具有最高可繞度的導線段。我們提議同時用多種的模型（如組合式〔combinatorial〕、解析式〔analytical〕及統計式〔stochastic〕的模型），並佐以廣泛的實驗，來探討此結構的設計與分析。由於結構與輔助工具(如繞線結構與繞線器）的設計，實爲相輔相成的兩項工作。導線段結構的品質須用繞線器來評估；

而繞線器的設計則須考慮結構的特性。因此，本項研究的成功將同時對 FPGA 的結構及其繞線器的設計有重要的貢獻。



圖一： Two major FPGA architectures. (a) Symmetric-array-based architecture. (b) Row-based

獻　背景和目的

自從 FPGA 於十餘年前問世以來[8]，由於其現場可程式化(field-programmable)的特性，使其在很短的時間內即成爲能夠同時滿足半導體市場之低成本、低風險、短設計週期及簡易設計變更等要求的最佳技術。一般而言，FPGA 的結構由邏輯模組(logic modules)和用以連結此邏輯模組的繞線資源(routing resources)所組成[5]。在邏輯模組內含有組合(combinational) 與序列(sequential)電路，用以製作各種邏輯函數。對稱陣列型(symmetric array-based) FPGA[3, 19, 32]的繞線資源包含水平與垂直的通道(channels)和可程式化開關(programmable switches)；而橫列型(row-based) FPGA[1, 16]的繞線資源則主要由橫列的通道和可程式化開關所組成。在這兩種主要的 FPGA 結構中，每條通道皆由一組軌道(tracks)所構成；而每條軌道又可細分成數個導線段(wire segments)。兩個相鄰的導線段間含有一個可程式化開關；藉由程式化這些開關，此相鄰的導線段得以連接而用來製作較長的通路(path)。使用 FPGA 製作邏輯電路，首先須切分電路，以便每個子電路皆能置入相關的邏輯模組中，然後再於各邏輯模組間作訊號的繞線。而 FPGA 繞線之達成即藉由控制可程式化開關以連接通道內的導線段。

在目前的兩種主要的 FPGA 結構中，以對稱陣列型最受歡迎。然而，相較於對橫列型導線段與可程式化開關的大量研究[10-12, 23-26, 31, 33]，目前對於對稱陣列型導線段結構的探討卻顯不足。此乃由於對稱陣列型導線段結構的高複雜度對其研究所造成之困擾所致。FPGA 的繞線通道含有各種不同長度的導線段[1, 32]。以較短的導線段作繞線需要使用較多的開關作連接；然而，以目前的技術所製成的可程式化開關皆有很高的電阻(resistance)和電容(capacitance)，此高電阻和電容會造成可觀的訊號延遲(delay)。反之，以較長導線段作繞線雖可降低開關的使用量，但易浪費部分導線段資源，而佔用較大的面積。而開關的數量若不足，則此 FPGA 的可繞度(routability)將會大幅降低。因此，爲了改進電路的速度，減低晶片的面積，並維持合理的可繞度，FPGA 的繞線通道通常含有各種不同長度的導線段；長導線段適用於需快速傳遞的訊號線，而短導線則用於較短的訊號以降低未繞經的導線資源浪費。此種速度、面積及可繞度的交互影響，即爲研究 FPGA 導線段設計(segmentation design)的最主要動機。

本計劃的目的在於建立一套有系統的方法，希望對於對稱陣列型 FPGA 導線段的結構設計與分析有所突破。如前所言，FPGA 的繞線資源包含導線段和可程式化開關；因此，對 FPGA 繞線資源的結構設計，須兩者兼顧。近年來，我們曾經提出有效的可程式化開關模型，並對其結構的設計與分析作出重要的貢獻。然而，目前工業界和學術界仍無法提出一套有系統而且令人信服的方法來分析對稱陣列型 FPGA 的導線段結構；因此，目前商品化的 FPGA，其導線段結構的設計仍是基於經驗與直覺，而非紮實的理論根基。

FPGA 導線段結構設計有三項相互競爭的考量：可繞度、面積及速度。因此，導線段結構設計的基本目標在於設計出能夠同時滿足面積及速度要求下，具有最高可繞度的導線段群。我們試圖從多種的模型（如組合式〔combinatorial〕、解析式〔analytical〕及統計式〔stochastic〕的模型）並佐以廣泛的實驗來探討此結構設計問題。（對於這些模型的探討，詳見表二十研究方法。）本計劃的最終目的則在於整合此結構的探討和我們之前對可程式化開關的研究，希望對於對稱陣列型 FPGA 的結構設計有重要的貢獻。

近年的研究顯示： FPGA 製作電路的可行性（feasibility）主要受限於繞線資源（而非邏輯資源）[4, 30]；而 FPGA 電路的效能最主要取決於繞線的速度（而非邏輯間的速度）[4, 28]。因此，繞線的結構實爲 FPGA 設計最關鍵的部分。良好的導線段結構不僅可增進用 FPGA 製作電路的可行性、提高 FPGA 電路的效能，更由於結構與輔助設計工具的交互影響，其對 FPGA 繞線器(router)的設計亦有極大的助益。

在早期的對稱陣列型FPGA中，其導線段僅有兩種長度：單位長(single)和全長(longline)（如 Xilinx XC2000系列的FPGA）[32]。但是隨著FPGA晶片密度的快速成長，其繞線資源的複雜度亦相對地提高以因應對可繞度、面積及速度的要求；

例如，近有二倍長（double）（如Xilinx XC4000E FPGA）及四倍長（quad）（如Xilinx XC4000EX FPGA）導線段的出現[32]。然而，目前工業界對導線段結構的設計方法仍是基於舊式的經驗與直覺；因此，導線段結構設計方法的突破，即成爲工業界和學術界所企盼的目標。

關於 FPGA 導線段的研究，目前幾乎集中於對橫列型結構的探討[17, 23, 26, 33]。Gamal 等人[17]首先對橫列型 FPGA 的導線段結構作分析，其認爲藉由適當的導線段設計，橫列型 FPGA 可達到與傳統的 standard cells 相當的可繞度。Roy 和 Mehendale [26]首先考慮用輔助工具，取代人工來作橫列型導線段的設計，而其所採用的方法爲根據所給定的分佈函數（distribution function）以決定導線段之長度及其在通道內的位置。Zhu 和 Wang [33] 延伸 Roy 和 Mehendale 的觀念，並改良導線段的模型；同時，他們亦製作一個橫列型 FPGA 的繞線器來評估設計的可繞度。之後，Pedram [23]等人利用解析的模型對橫列型 FPGA 導線段的結構作深入的分析，並提出與[17]對橫列型 FPGA 可繞度相同的看法。

目前對於對稱陣列型 FPGA 繞線結構的研究，皆集中於可程式化開關部份。Rose 和 Brown [24]首先對開關模組的彈性係數(flexibility)和可繞度的關係，以廣泛的實驗作探討。其由實驗的觀察，發現一些適合對稱陣列型 FPGA 開關模組的結構參數；但是，他們並無法提出理論的解釋。我們於近年提出一套解析的模型，藉由此模型的分析，我們發現完備的整組最低成本的「萬用開關模組」（universal switch modules），並修正及解釋 Rose 和 Brown 的觀察結論[11, 12]。相較於對可程式化開關的大量研究[7, 10-12, 24, 27, 31, 34]，目前對於對稱陣列型導線段的探討卻極爲匱乏，Zhu 等人[34]曾提出利用開關模組的設計來規劃對稱陣列型導線段結構的觀念，但並未實際進行導線段設計。

結構（architecture）與輔助工具（CAD）（如繞線結構與繞線器）的設計，乃爲相輔相成的兩項工作。導線段結構設計的良窳需用繞線器來評估；而繞線器的設計則需考慮結構的特性。因此，除導線段結構設計外，我們亦需探討繞線器的製作（此爲本計畫的附帶工作之一）。關於 FPGA 繞線器製作的文獻極多，重要者如[17, 18, 33]（橫列型 FPGA 繞線）和[2, 6, 9, 13-15, 20-21, 27]（對稱陣列型 FPGA 繞線）。然而，目前大部分對稱陣列型 FPGA 繞線器祇考慮單一導線段長度的模型；因此無法直接應用於本計畫的實驗。而由於模型的差異，對現有考慮多種導線段的繞線器[14, 15]，我們仍需作近一步的評估與修改。

步、研究方法

在本研究中我們以多種的模型（如組合式〔combinatorial〕、解析式〔analytical〕及統計式〔stochastic〕的模型），並佐以廣泛的實驗來探討對稱陣列型導線段結構的設計與分析，而且也獲得了相當不錯的成果，已經發表於國內與國際知名的會議(見 A.1 和 A.2)。關於 FPGA 繞線器的設計，我們也提出新的的解決方法，它能夠因應越來越複雜的 FPGA 結構，考量不同長度的導線段（目前學術界的 FPGA 繞線器大多只考慮單一導線段長度），同時增進繞線的效能與可繞度，來處理 FPGA 的繞線問題。(此部份成果請參見 A.3)

五、成果(Publications from this Project)

A.1 Yao-Wen Chang, Jai-Ming Lin, and D. F. Wong, "Graph Matching-Based Algorithms for FPGA Segmentation Design," *in Proc. of IEEE/ACM Int. Conf. on Computer Aided Design,* 1998. (submitted *IEEE Trans. On Computer-Aided Design*)

A.2 Yao-Wen Chang and Jai-Ming Lin, "Channel Segmenation for FPGA Design," *in The 9th VLSI Design/CAD Symposium,* Taiwan, Aug. 1998.

A.3 Kai Zhu, Yao-Wen Chang, and D.F. Wong, "Timing-Driven Routing for Symmetrical Array-Based FPGAs," *in Proc of IEEE Int. Conf. on Computer Design*, Oct. 1998. (To appear in *ACM Trans. On Design Automation of Electronic Systems,* Arp. 2001.)

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