LPCVD 製程設備之加熱及進氣系統設計、流場模擬與系統整合及建立 **(Ⅱ)**（子計畫一）

Heating and Gas Feeding System Design, Flow Simulation, Design and Establishmentof a LPCVD Process Equipment (Ⅱ)

計畫編號：NSC 87-2218-E-009-006
執行期限：86 年 8 月 1 日至 87 年 7 月 31 日
主持人：林清發教授　交通大學機械系

一、中文摘要

本三年期研究計畫(85 年 8 月至 88 年 7 月)，主要針對晶片製程上常用之 LPCVD 反應爐，設計新的 lamp 加熱系統及反應氣體進氣系統，以改進晶片溫度之均勻性及晶片上反應氣體濃度之均勻性。同時，我們將以 numerical model 來模擬 LPCVD 反應爐內之流場分佈。由其他子計畫所獲得之輻射熱傳分佈、晶片內之熱應力分佈與加熱燈之安排對製程影響等結果，將與本計畫之結果整合在一起來設計整個 LPCVD 反應爐。依據此一改良之設計，我們將建立一新的 CVD 反應爐。此一反應爐將用以成長 Ta_2O_5 薄膜。由此成長之薄膜性質之優劣，將回饋至反應爐設計，以改進反應爐。

在本年度，第二年計畫裡(86 年 8 月至 87 年 7 月)，我們已對第一年所建造的反應器進行詳細量測及數值模擬。結果顯示熱浮力所驅動之流體轉動非常強。加入 showerhead 及降低爐體壓力可有效降低浮力效應，而利用等溫銅板可使晶圓之溫度分佈較均勻。

關鍵詞：LPCVD 反應爐、加熱設計、流力設計

Abstract

In this individual three-year research project (August 1996 to July 1999) we intend to improve the uniformity of the temperature and gas concentration over the entire wafer through new lamp heating system and gas delivery system design in a LPCVD reactor. Meanwhile, a numerical model will be proposed to simulate the gas flow in the LPCVD reactor. Results for the thermal radiation distribution, thermal stress in the wafer and influences of the heating lamp arrangement from the individual projects will be combined with those from this individual project to design the whole LPCVD reactor. Based on this improved design, a new LPCVD reactor will be established. Tests will be conducted to use this reactor to grow a Ta_2O_5 thin film. The data for the grown film will be fed back to improve the reactor.

In the second year of the study (August 1997 to July 1998) the flow and thermal characteristics in the reactor established in the first year were investigated in detail through numerical modeling and experimental measurement. The results indicate that the buoyancy driven recirculating flow is rather strong. Using showerhead and lowering the reactor pressure can significantly reduce the buoyancy effects. Besides, the wafer

temperature uniformity can be smoewhat improved by the thick isothermal copper plate.

Keywords： LPCVD Reactor Heating Design, Flow Design

二、計畫緣由與目的

近幾年來由於微電子元件之日益急速微小化及晶片功能之大幅提昇，積體電路已由 VLSI 發展到 ULSI，晶片也將由 8 吋擴大至 12 吋,因此如何精確地控制熱流條件使在大晶圓上成長的各類薄膜能達到均勻厚度、純度、線寬等之要求，以及減低晶片內之熱應力等，實為目前急需解決之重要問題。本子計畫之主要目的即在改進 IC 晶片製程之加熱系統及反應氣體進氣道設計，使大晶圓之溫度能均勻分佈，反應氣體在整個晶片上之濃度亦均勻分佈。同時亦將進行詳細 LPCVD 流場分析、計算，以改進熱流設計。另外，也將結合其他子計畫之成果，對於整個 LPCVD 系統進行整體設計。依此新設計建立一套 LPCVD 爐，對於建立本土 LPCVD 製程設備技術之提昇甚為重要。

LPCVD 為 IC 晶片製造之重要製程設備之一，先進國家在這方面已有甚多之研究，但國內做的並不多，尤其是在建立 LPCVD 反應爐設備方面，落後甚多。過去的 IC 晶片製造大多為 resistance heating,較難精確製造細微線路,且能源消耗較多。近來所發展之單一大晶片的 rapid lamp heating 則較省能，微細線路控制較好，但只要有少許之溫度不均勻，易造成薄膜厚度不均勻，且晶片易受熱應力而變形或破裂。

過去的 LPCVD 反應爐大多使用 resistance heating 加熱，主要分成水平及垂直兩類反應爐，有關此方面的研究甚多。有關 rapid lamp heating LPCVD 製程研究，近年來國外已有一些，但詳細之 LPCVD 反應爐設計及建造資料則甚難在公開文獻上獲得,大多列為公司機密。因此，國內欲建立 LPCVD 反應爐建造技術，必需靠自己慢慢建立。

三、結果與討論

我們在第一年所建造之反應爐的示意圖及相片，如圖一所示。在本年度裡，本子計畫所獲得之主要結果，討論如下：

(1)熱浮力所驅動之 flow recirculation 相當的複雜，如計算（圖二）及實驗流場觀測（圖三）所示。為了減弱 recirculating flow，我們可加入 showerhead 。另外亦可降低爐內壓力或爐體高度。

(2)於晶圓下方換置一厚的等溫銅板對於改善晶圓溫度分佈之均勻性有相當的幫助，我們所量測之晶片上五點之溫度隨時間變化（在加熱過程及不加熱過程），如圖四所示。顯示晶片上之溫差已較目前的爐子好。

四、計畫成果自評

第二年之詳細流場分析及實驗觀測所提供之資料對於我們瞭解第一年所建造之反應爐有很大幫忙。此一爐子之優缺點對第三年要建造之改良式反應爐極為重要。

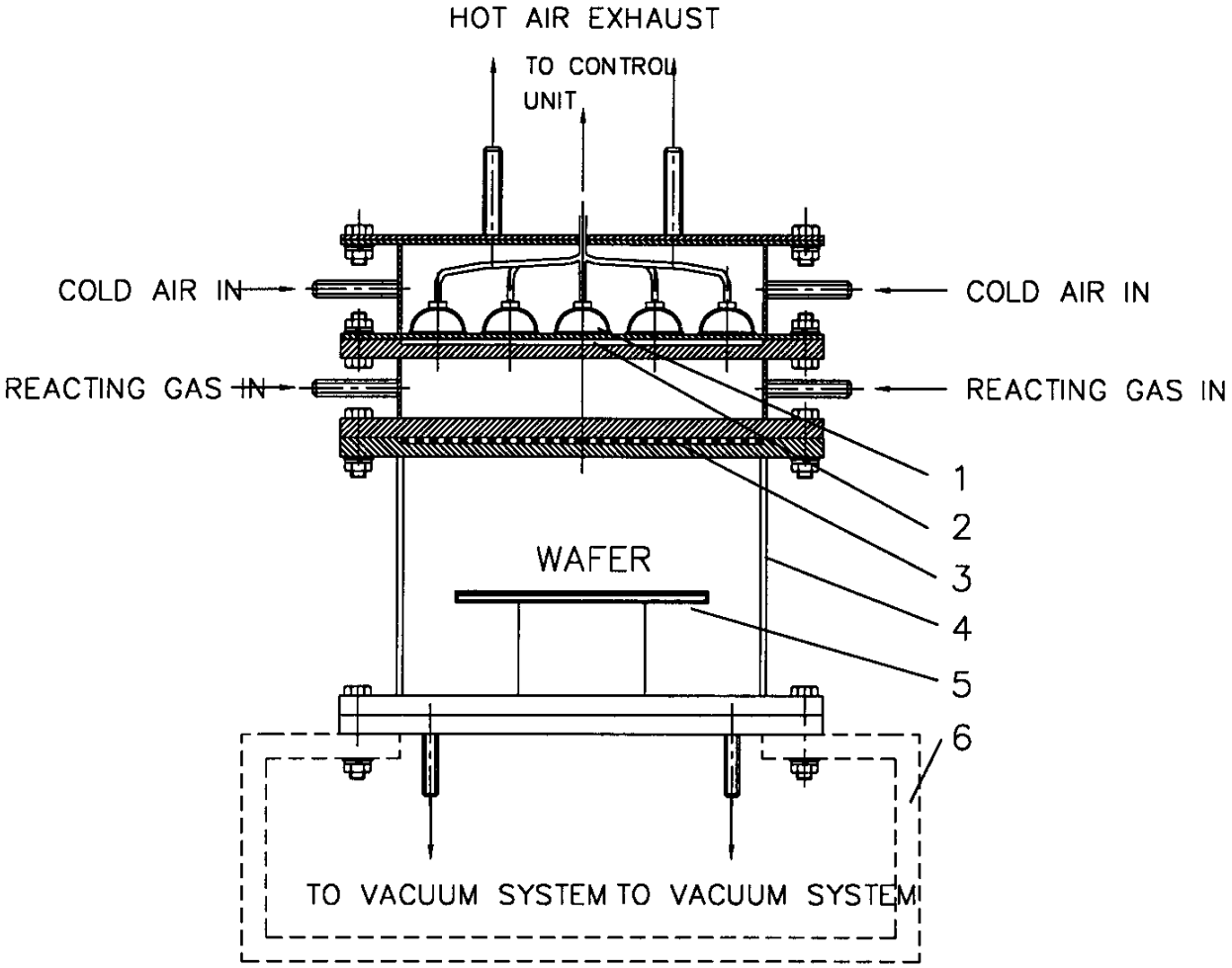
五、參考文獻

1. M.Hierlemann, A. Kersch, C. Werner,

and H. Schafer, 1995, A Gas-Phase and Surface Kinetics Model for Silicon Epitaxial Growth with SiH2Cl2 in an RTCVD Reactor, J.Electrochem . Soc., Vol. 142, No. 1, 259-266 .

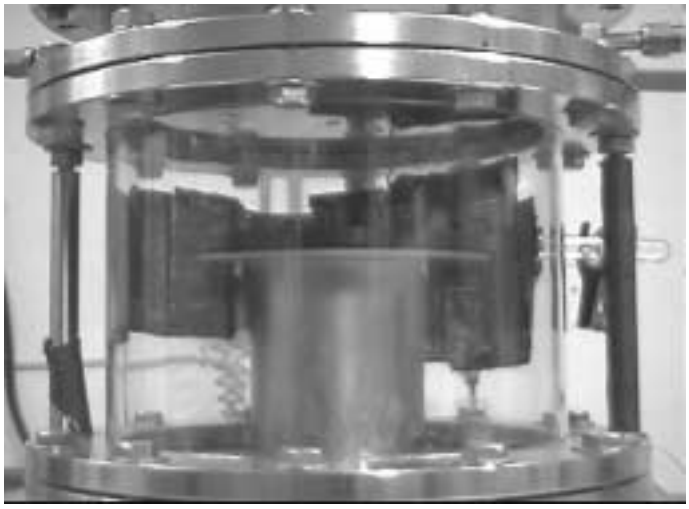
2. Mehmet C.Ozturk, F.Yates Sorrell, Jimmie J. Wortman, F. Scott Johnson, and Douglas T. Grider,1991, Manufacturability Issues in Rapid Thermal Chemical Vapor Depsition, IEEE Transfers on Semiconductor Manufacturing, Vol. 4, No. 2, 155-165 .
3. S.Reynolds, D.W.Vook, and J.F.Gibbons, 1986, Limited Reaction Processing: Growth: of III-V Epitaxial Layers by Rapid Thermal Metalorganic Chemical Vapor Deposition, Appl. Phys. Lett., Vol. 49, No. 25, 1720-1722.
4. Mahesh K. Sanganeria, Katherine E. Violette, and Mehmet C. Ozturk, 1995, Boron Incorporation in Epitaxial Solicon Using Si2H6 and B2h6 in an Ultrahigh Vaccum Rapid Thermal Chemical Vapor Deposition Reactor, J. Electrochem. %c, Vol. 142, No. 1,285-289.
5. Anthony J. Toprac, Isaac Trachtenberg, and Thomas F. Edgar, 1994, A Predictive Modelfor the Chemical Vapor Deposition of Polysilicon in a Cold Wall, Rapid Thermal system, J. Electrochem . Soc, Vol. 141, No. 6, 1658-1663.
6. J. Mercier, J . L . Regolini, D. Sensahel, and E. Scheid, 1989, Kinetic Aspects of Selective Epitaxial Growth Using a Rapid Thermal Processing System, Journal of Crystal Growth 94(1989) 885-894.
7. Yasuo Uoochi, Akira Tabuchi ,and Yuji Furumura, 1990,Spin-on Glass Curing by Rapid Thermal Annealing , J. Electrochero··Sec., Vol. 137, No. 12, 3923-3925.
8. Ronald K . Sampson and Hisham Z. Massoud, 1993, Resolution of Silicon Wafer Temperature Measurement by In Situ Ellipometry in a Rapid Thermal Processor, J . Electrochem. Soc., Vol. 140, No. 9, 2673-2678.
9. R.K.Sampson, E;. A. Conrad, E. A. Irene, and H. Z. Massound, 1993, Simulaneous Silicon Wafer Temperature and Oxide Film Thickness Measurement in Rapid-Thermal Processing Using Ellipornetry, J. Electrochem. Soc., Vol.140, No. 6, 1734-1743.
10. R.K.Sampson K. A. Conrad, H. Z. Massound, and E. A. Irene, 1994, Substrate Doping and Microroughness Effects in RTP Temperature Measurement by in Situ Ellipsometry , J . Electrochem. Soc., Vol. 141, No. 3, 737-741.
11. E. Kobeda, M . Kallam, and C. M. Osburn, 1991, Rapid Thermal Annealing of Low-temperature Chemical Vapor Deposition Oxides, J. Electrochem . Soc., Vol. 138, No · 6, 1846-1849.
12. Mehrdad M. Moslehi, 1989, processing Uniformity and Slip Dislocation Patterns in Linerly Ramped-Temperature Transient Rapid Thermal Processing of Silicon, IEEE Transactions Semiconductor

Manufacturing, Vol. 12, No. 4, 130-140.
13. R.Deaton and H. Z. Massond, 1991, Effect of Thermally Induced Stresses on The Rapid-Thermal Oxidation of Silicon, J. Appl. Phys, Vol. 70, No. 7, 3588-3592.
14. Kare Maex, 1991, Rapid Thermal Processing and Thin Film Technologies, Microelectmic Engineering I5(1991) 467-474.
15. M. J. Hart and A. G. R. Evans, 1988, Rapid Thermal Processing in Semiconductor Technology, Semicond. Sci. Technol. 3(1988) 421-436.
16. J. C. Gelpey, M. C. Ozturk, R. P. S. Thakur, A. T. Fiory, F. Roozeboom, ed., Rapid Thermal and Integrated Processing V, Material Research Society Symposium Proceedings, Vol. 429 (1996) Pittsburgh.



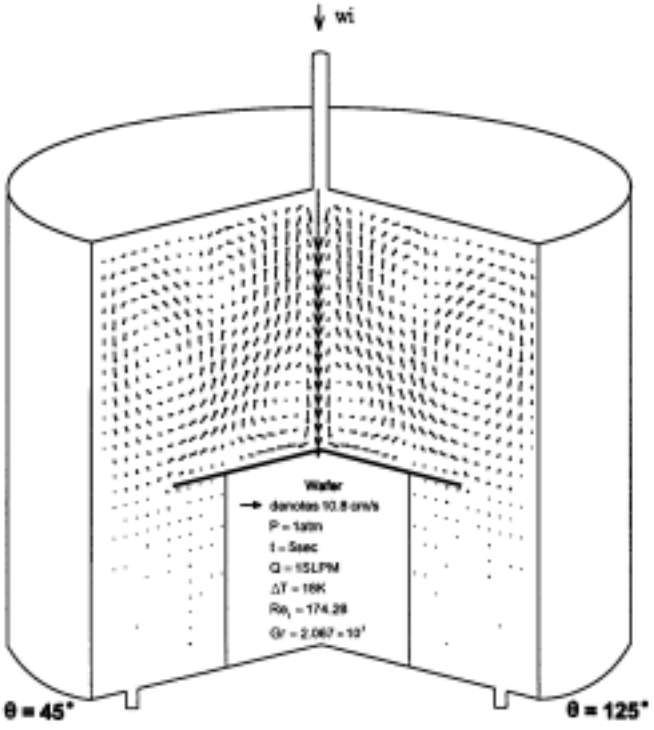
1 -- HEATING LAMPS
2 -- CRYSTAL HOLDER
3 -- SHOWER HEAD
4 -- PYREX REACTOR BODY
5 -- SUSCEPTOR
6 -- REACTOR HOLD STRUCTURE

圖一. (a)Schematic diagram, and (b)photos for the reactor

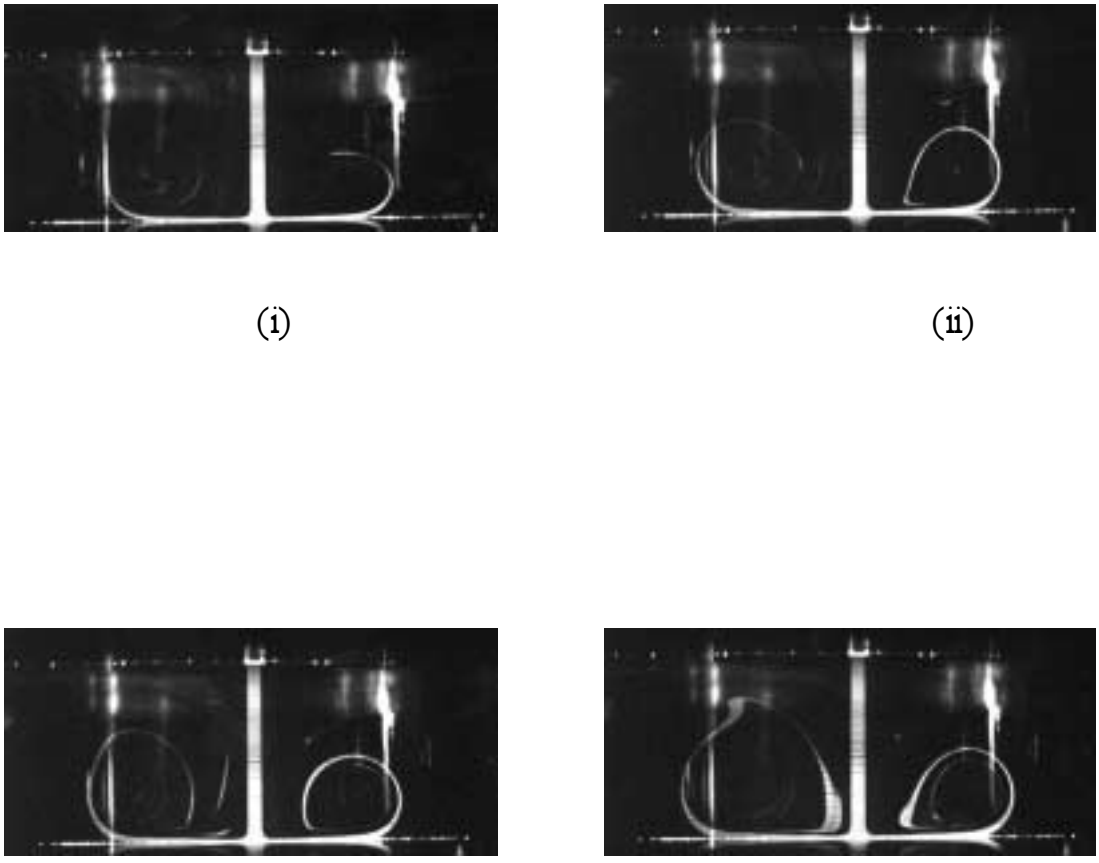


(b)

圖一. **continued**



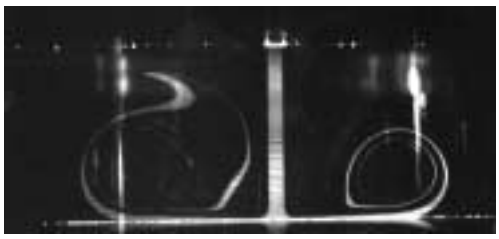
圖二. Velocity vector maps on the planes : = 45°& 125°at t=5 sec for Q=1 SLPM, T_f=313 K and P=1 atm (Re_j=174.28, Gr=2.067×10^7, w_I=33.16 cm/s)



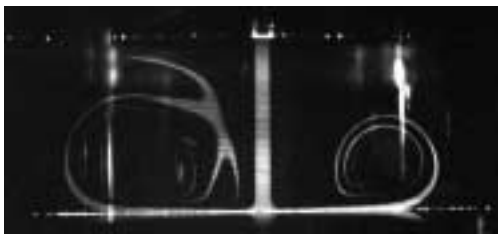
(i) (ii)

(iii) (iv)

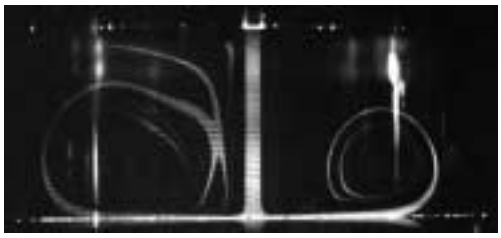
圖三. Photographs of the transient flow pattern for× T = 3× for 1 SLPM and P=1 atm (Re_j=174.28, Ra=1.51×10^7) at t = (i) 0 sec (ii) 1 sec (iii) 2 sec (iv) 3 sec (v) 4 sec (vi) 5 sec (vii) 6 sec (viii) 7 sec



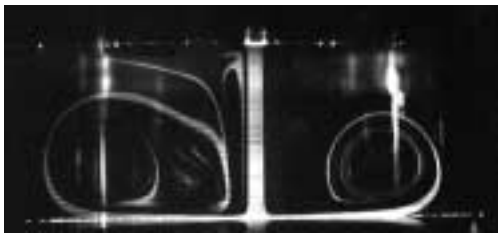
(v)



(vi)

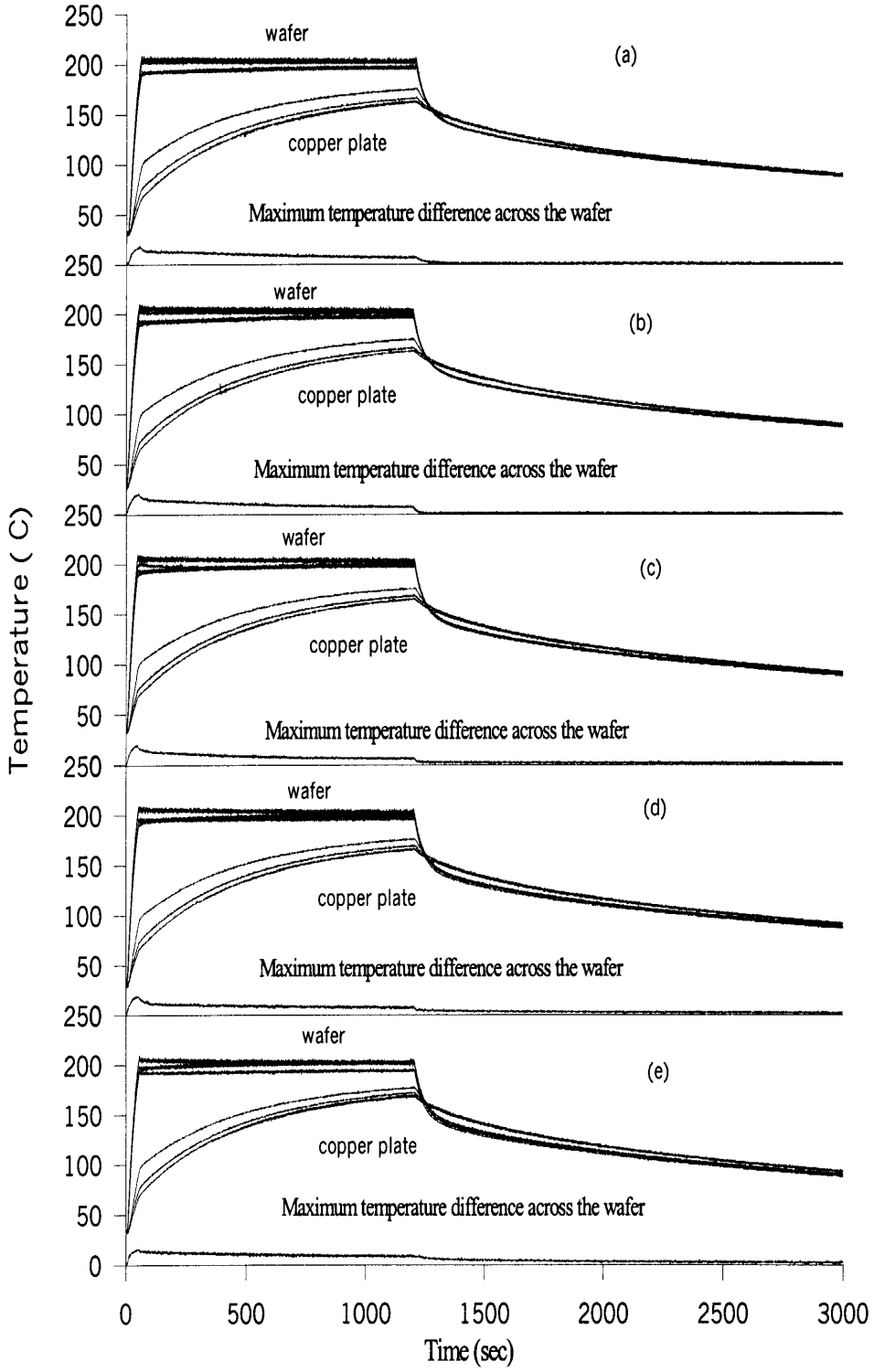


(vii)



(viii)

圖三. Continued



圖四. The wafer temperature at selected points and the maximum temperature differences across the wafer during the entire heating process for Ts=200 × with flange copper plate and for (a)Qin=0 SLPM, (b)Qin=1 SLPM, (c)Qin=2 SLPM, (d)Qin=3 SLPM, and (e)Qin=5 SLPM.