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Improvement of light output in GaN-based power chip light-emitting diodes with a nano-rough surface by nanoimprint lithography

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Abstract

The enhancement of light extraction of gallium nitride (GaN)-based power chip (PC) light-emitting diodes (LEDs) with a *p*-GaN rough surface by nanoimprint lithography (NIL) is presented. At a driving current of 350 mA and a chip size of 1 mm × 1 mm, the light output power of the PC LEDs with a *p*-GaN rough surface (etching depth from 130 to 150 nm) showed an enhancement of 24% on wafer when compared with the same device without NIL. Current–voltage results indicated an ohmic contact by the increase in the contact area of the nano-roughened surface at 200 mA. This paper offers a promising potential for enhancing the output powers of commercial LEDs.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Recently, the development in high-brightness gallium nitride (GaN)-based light-emitting diodes (LEDs) being implanted in flat-panel displays has made more possible for the LEDs to be used in many display technologies [1, 2]. To further reduce the cost and enhance the performance of these LEDs, there is always a great need to improve the internal as well as external quantum efficiency in order to further increase their light output power. Furthermore, the external quantum efficiency of GaN-based LEDs is low because the refractive index of the nitride epitaxial layer differs greatly from that of the air. The refractive indices of GaN and air are 2.5 and 1.0, respectively. Thus, the critical angle at which light generated in the InGaN/GaN-active region can escape is approximately $[\theta_c = \sin^{-1}(n_{\text{air}}/n_{\text{GaN}})] \sim 23^\circ$, which limits the external quantum efficiency of conventional GaN-based LEDs to only a

few percent [3]. The light from LEDs can be enhanced either through the sample surface or through the sidewalls of the chip. Research into improving the light extraction efficiency (external quantum efficiency) and brightness in the LEDs [3–8] has been intense. Recently, we reported an increase in the extraction efficiency of GaN-based LEDs by surface roughening [7, 8]. All these processes allow the photons generated within the LEDs to find the escape cone, by multiple scattering from a rough surface.

The insertion of a nano-rough pattern that can control the propagation of photons has become more important. To fabricate the nanosized pattern, e-beam lithography (EBL) [9, 10], laser interference lithography (LIL) [11] and nanoimprint lithography (NIL) [12, 13] have been used. However, EBL and LIL techniques have a low throughput and cannot be applied for the mass production of LED devices. Compared with EBL and LIL, NIL is one of the

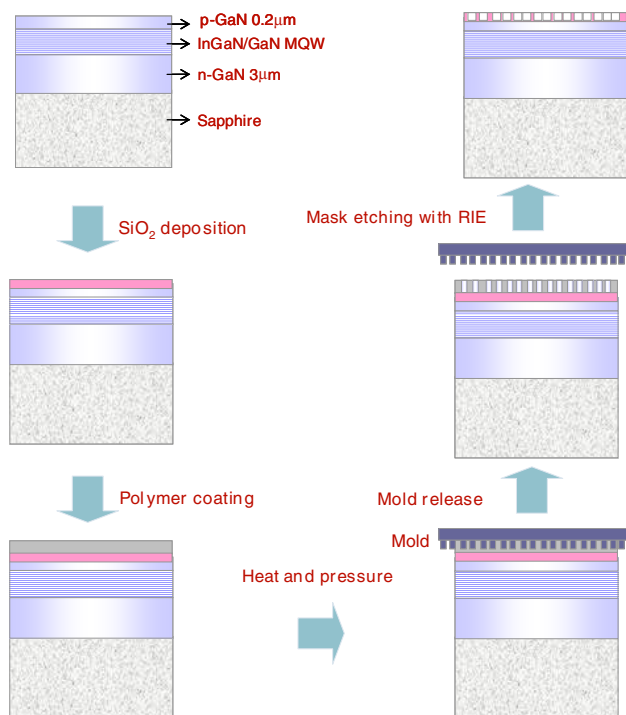


Figure 1. Process flow schematic diagram for nanoimprint lithography.

most promising technologies for nanosized pattern fabrication due to its high resolution and high throughput patterning capability with an extremely low cost for developing LED devices [13]. This investigation reports the production of GaN-based LEDs with a nano-roughened surface by NIL. As a result, the light output efficiency of an LED with a nano-roughened surface (etching depth from 130 to 170 nm) was significantly higher than that of a conventional LED without a roughened surface. Additionally, the current–voltage (I – V) measurements demonstrate that the forward voltage of an LED with a nano-roughened surface was lower than that of a conventional LED at 200 mA from the same wafer with standard device processing.

2. Experiments

GaN-based LED samples were grown by metal-organic chemical vapor deposition (MOCVD) with a rotating-disk reactor (Emcore D75TM) on a c -axis sapphire (0001) substrate at a growth pressure of 200 mbar. The LED structure consists of a 50 nm thick GaN nucleation layer grown at 500 °C, then a 2 μ m undoped GaN buffer layer grown at 1050 °C, a 3 μ m thick Si-doped GaN layer grown at 1050 °C, an unintentionally doped InGaN/GaN multiple quantum well (MQW) active region grown at 770 °C, a 50 nm thick Mg-doped p-AlGaIn electron-blocking layer grown at 1050 °C, a 0.2 μ m thick Mg-doped p-GaN contact layer grown at 1050 °C. The MQW active region consists of five periods of 3 nm/7 nm thick In_{0.15}Ga_{0.85}N/GaN quantum well layers and barrier layers. Figure 1 is a detailed process flow schematic

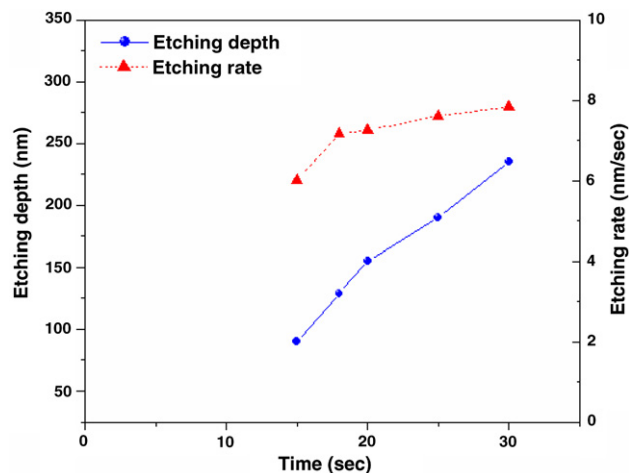


Figure 2. The etching rate of the p-GaN layer as a function of the ICP-RIE etching time.

diagram for our NIL. Firstly, the 50 nm SiO₂ was deposited onto the sample surface by plasma-enhanced chemical vapor deposition (PECVD). Secondly, we spin-coated a polymer layer on top of the SiO₂. Thirdly, we placed a patterned mold onto the dried polymer film. By applying high pressure, we heated the LED samples to above the glass transition temperature of the polymer. Fourthly, the LED samples and the mold were then cooled down to room temperature to release the mold. Finally, we used reactive-ion etching (RIE) with CF₄ plasma to remove the residual polymer layer and transferred the pattern onto SiO₂.

By inductively coupled plasma RIE (ICP-RIE), we partially etched the p-GaN surfaces of the LED samples using Cl₂/Ar as the etching gas. The etching gases Cl₂ and Ar were introduced into the reactor chamber through independent electronic mass flow controllers (MFCs) that could control the flow rate of each gas with an accuracy of about 1 sccm (standard cubic centimeters per minute). An automatic pressure controller (APC) was placed near the exhaust end of the chamber to control the chamber pressure. Figure 2 shows the etching rate of the p-GaN layer as a function of ICP-RIE etching time. The etching rate of the p-GaN layer using the ICP etching condition, Cl₂/Ar = 10/25 sccm with the ICP source power, bias power set at 200/200 W and chamber pressure of 2.5 mTorr, was determined to be approximately 7.5 nm s⁻¹. The etching depth increased from 80 to 235 nm with the increasing etching time from 15 to 30 s. The ICP etching process for PC LEDs was used to form rough surface with four different etching times (LED I: 18 s, LED II: 20 s, LED III: 22 s and LED IV: 25 s). We then used a buffer oxidation etchant (BOE) to remove the residual SiO₂ layer.

Afterward, the conventional LED and the LED with a nano-rough surface by NIL were fabricated using the standard process (three mask steps) with a mesa area (950 × 950 μ m²). Firstly, the 0.52 μ m SiO₂ was deposited onto the sample surface by PECVD. Photo lithography was used to define the mesa pattern after wet etching of SiO₂ by a BOE solution. The mesa etching was then performed with Cl₂/Ar

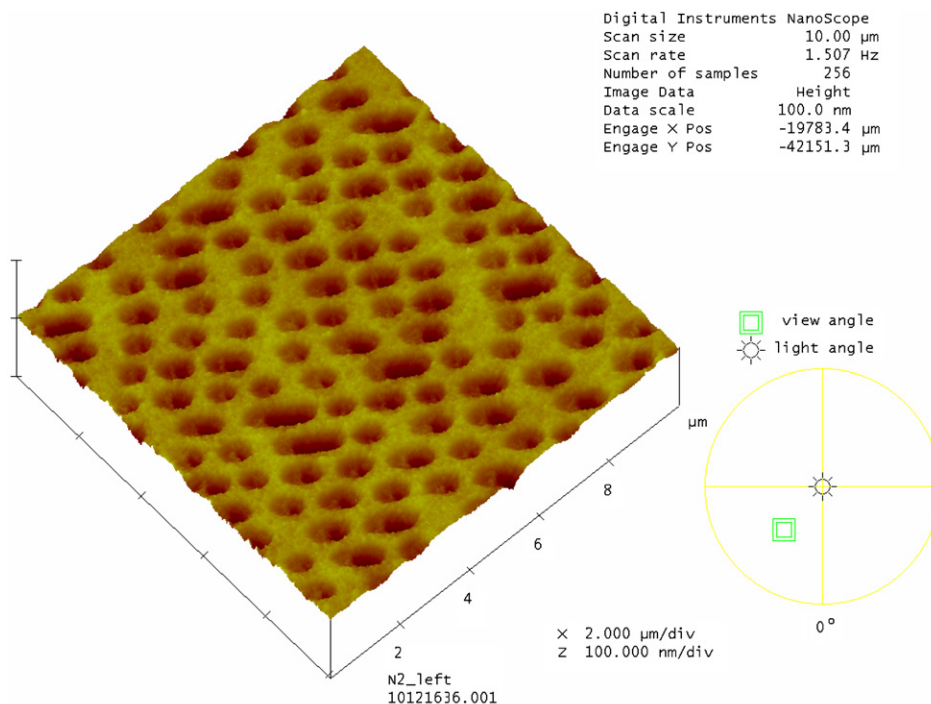


Figure 3. The AFM image of LEDs by nanoimprint lithography without the RIE etching process.

as the etching gas in an ICP-RIE system transferred the mesa pattern onto the n-GaN layer. A 300 nm thick ITO layer was subsequently evaporated onto the LED samples surface. The ITO layer had a high electrical conductivity and a high transparency. The metal pad layers were patterned by a lift-off procedure and deposited onto samples by electron beam evaporation. Cr/Pt/Au (20/30/1000 nm) were used for the p- and n-type electrode. For comparison, PC LEDs with and without a p-GaN nano-rough surface by NIL were chosen from the same wafer location possessing the same internal quantum efficiency and the same emitting wavelength.

Figure 3 shows the AFM pattern image of PC LEDs with a nano-rough surface by NIL without RIE etching. The AFM image shows that the nano-hole dimension and the density of the PC LEDs mesa surface were approximately 200–500 nm and $1 \times 10^8 \text{ cm}^{-2}$, respectively, and the polymer layer height was approximately 0.15 μm .

3. Results and discussion

The light output was detected by a calibrated integrating sphere with a Si photodiode on the LED wafer device. Figure 4 shows the typical I – V characteristics. It was found that the measured forward voltages at an injection current of 350 mA at room temperature for the conventional LED, LED I, LED II, LED III and LED IV were 4.56, 4.58, 4.62, 4.66 and 2.76 V, respectively. In figure 4, the I – V results indicated that nano-roughening facilitates p-type contact, resulting in an ohmic contact by the increase in the contact area of the nano-roughened surface below 200 mA (because of the better ohmic contact with the nano-roughened surface in the current range

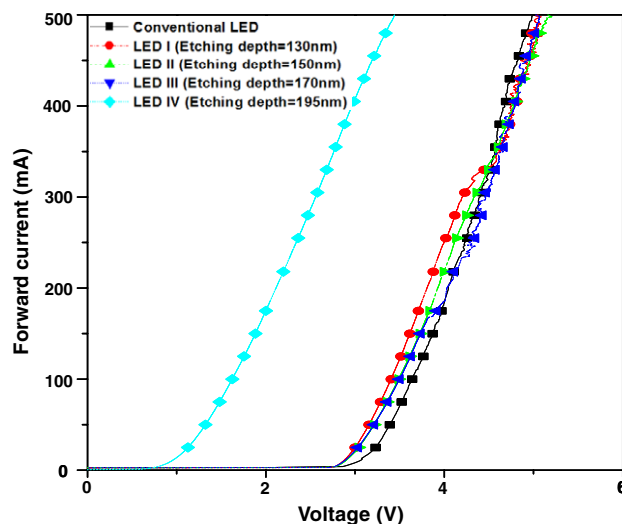


Figure 4. Current–voltage (I – V) measurement characteristics of PC LEDs with a nano-rough surface by nanoimprint lithography and conventional LEDs, respectively.

from 10 to 200 mA). However, over 300 mA the nano-rough surface by NIL indicated that there is heating and charging damages for the fabrication process of NIL during the ICP etching process. Further, the forward voltage of LED IV is lower as the etching depth of the p-AlGaIn layer induces the leakage current.

The intensity–current (L – I) characteristics of the five different types of LEDs are shown in figure 5. We clearly observed that the output powers of the LED I (etching

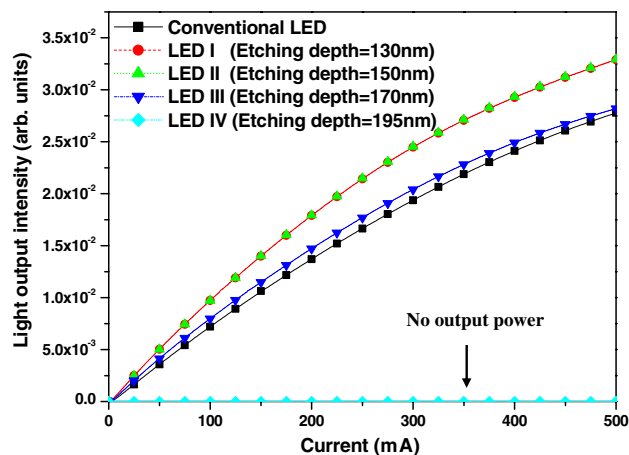


Figure 5. Intensity–current (L – I) characteristics of PC LEDs with a nano-rough surface by nanoimprint lithography and conventional LEDs, respectively.

depth = 130 nm) and LED II (etching depth = 150 nm) were larger than that of the conventional LEDs. At an injection current of 350 mA, the light output power of the PC LEDs with a nano-rough surface by NIL on wafer shows enhancement by 24% compared to the PC conventional LEDs. The 24% improvement in the light emission reported here compares very well with the 25% improvement reported by Cho *et al* [14]. This enhancement is attributed to the higher scattering effect of PC LEDs with a nano-rough surface by NIL (etching depth from 130 to 150 nm) when compared to conventional LEDs.

4. Conclusion

In conclusion, GaN-based PC LEDs with a nano-rough surface by NIL were demonstrated and fabricated. At a driving current of 350 mA and a chip size of 1 mm × 1 mm, the light output power of PC LEDs with a nano-rough surface by NIL showed an enhancement of 24% when compared with conventional LEDs. I – V properties indicated that nano-roughening facilitates p-type contact, resulting in an ohmic contact by the increase in the contact area of the nano-roughened surface below 200 mA.

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