Effects of interfacial sulfidization and thermal annealing on the electrical properties of an atomic-layer-deposited Al 2 O 3 gate dielectric on GaAs substrate

Chao-Ching Cheng, Chao-Hsin Chien, Guang-Li Luo, Chun-Hui Yang, Ching-Chih Chang, Chun-Yen Chang, Chi-Chung Kei, Chien-Nan Hsiao, and Tsong-Pyng Perng

Citation: Journal of Applied Physics **103**, 074102 (2008); doi: 10.1063/1.2901167
View online: http://dx.doi.org/10.1063/1.2901167
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/103/7?ver=pdfcov
Published by the AIP Publishing

Effects of interfacial sulfidization and thermal annealing on the electrical properties of an atomic-layer-deposited Al_2O_3 gate dielectric on GaAs substrate

Chao-Ching Cheng,[1] Chao-Hsin Chien,[1,2,a)] Guang-Li Luo,[2] Chun-Hui Yang,[2] Ching-Chih Chang,[1] Chun-Yen Chang,[1] Chi-Chung Kei,[3] Chien-Nan Hsiao,[3] and Tsong-Pyng Perng[4]

[1]*Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan 300, Republic of China*
[2]*National Nano Device Laboratory, Hsinchu, Taiwan 300, Republic of China*
[3]*Instrument Technology Research Center, National Applied Research Laboratories, Hsinchu, Taiwan 300, Republic of China*
[4]*Department of Material Science and Engineering, National Tsing-Hua University, Hsinchu, Taiwan 300, Republic of China*

(Received 15 September 2007; accepted 22 January 2008; published online 1 April 2008)

In this study we investigated the interfacial chemistry occurring between an atomic-layer-deposited Al_2O_3 high-*k* film and a GaAs substrate and the impact of sulfidization and thermal annealing on the properties of the resultant capacitor. We observed that sulfide passivation of the Al_2O_3/GaAs structure improved the effect of Fermi level pinning on the electrical characteristics, thereby providing a higher oxide capacitance, smaller frequency dispersion, and reduced surface states, as well as decreased interfacial charge trapping and gate leakage currents. Photoemission analysis indicated that the $(NH_4)_2S$-treated GaAs improved the quality of the as-deposited Al_2O_3 thin film and preserved the stoichiometry of the dielectric during subsequent high-temperature annealing. This behavior was closely correlated to the diminution of GaAs native oxides and elemental arsenic defects and their unwanted diffusion. In addition, thermal processing under an O_2 atmosphere, relative to that under N_2, decreased the thickness of the Al_2O_3 gate dielectric and relieved the gate leakage degradation induced by metallic arsenic; as a result, superior dielectric reliability was attained. We discuss the underlying thermochemical reactions that account for these experimental observations. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2901167]

I. INTRODUCTION

Presently, GaAs materials are used widely in such applications as optoelectronic devices, photodiodes, high-electron-mobility transistors, and other high-frequency devices. In attempts to obtain superior performance rivaling or exceeding that of transistors on traditional Si-based substrates, various high-*k* gate dielectrics have been examined on high-mobility III-V substrates, especially GaAs- and InSb-based compound materials.[1,2] Studies into competitive insulators on compound semiconductors and efficient passivation methods have been performed for more than four decades; the poor quality of the insulator-substrate interface has been the foremost obstacle hindering the realization of III-V metal oxide semiconductor (MOS) devices. In addition to SiO_2 and Si_3N_4,[3] atomic-layer-deposited (ALD) Al_2O_3,[4] $(Gd,Ga)_2O_3$,[5] and HfO_2 high-*k* dielectrics[6] are also potential candidates for use on GaAs substrates. Surface sulfide treatment and the use of ultrathin Si or Ge interfacial passivation layers are both practical techniques for improving electrical characteristics. The passivation of GaAs surfaces with Na_2S or ammonium sulfide $[(NH_4)_2S]$ prior to deposition of the gate dielectric has been reviewed comprehensively;[7,8] the improvement in the device performance depends strongly on the sulfide treatment procedure.[9] The *in situ* deposition of several Si or Ge monolayers on GaAs (Refs. 10 and 11) can reduce the interfacial state density to approximately 10^{10}–10^{11} $cm^{-2}\,eV^{-1}$; this passivation technique has received renewed interest in recent years.[12,13] Subsequent thermal annealing can further improve the quality of insulator films deposited on GaAs.[14] Meanwhile, during high-temperature processing it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides; these processes lead directly to electrical deterioration in GaAs MOS capacitors.[15] The impact of rapid thermal annealing on the properties of various high-*k*/GaAs structures has been studied previously;[16] the gas used in the annealing process influences the thermochemical mechanism as well as the interfacial quality.[17] Nevertheless, correlations between these thermal reactions and the MOS performance have not been established in detail. In this study, we examined the material and electrical characteristics of ALD-Al_2O_3 thin films deposited on an $(NH_4)_2S$-treated GaAs surface and then monitored the impact of thermal annealing processing. The nature of the annealing environment also affected the electrical properties; this behavior could be interpreted by considering the latent thermodynamic mechanisms, which we identified from the physical analyses.

II. EXPERIMENTAL

n-Type GaAs substrates having a doping concentration of approximately 1×10^{18} cm^{-3} (resistivity <0.01 Ω cm)

a)Electronic mail: chchien@faculty.nctu.edu.tw.

were first rinsed in acetone (ACE) and de-ionized (DI) water for 1 and 5 min, respectively. Subsequently, dilute HCl solution (HCl/DI water, 1:10) was used to etch the surface native oxides. After wet chemical cleaning, the samples were dipped into aqueous ammonium sulfide solution $[(NH_4)_2S/DI$ water, 1:50] for 30 s or 30 min to passivate the GaAs surfaces prior to deposition of the dielectric. The Al_2O_3 thin films were deposited in the ALD system while maintaining the substrate temperature at 300 °C. Trimethylaluminum $[Al(CH_3)_3]$ and H_2O were chosen as the metal source and oxidant, respectively; they were pulsed alternately into the reactor for 1 s per pulse, separated by a N_2 purge of 10 s to remove redundant reactants. The deposition rate was approximately 1.0–1.1 Å s^{-1}. For comparison, the as-deposited Al_2O_3 dielectric films were subjected to post-deposition annealing (PDA) for 10 s at 600 °C in either a N_2 or O_2 ambient. The rapid thermal annealing (RTA) system was purged cyclically by pumping down to 25 torr and refilling the feed gas; the chamber pressure was then maintained at 1 atm during annealing after flushing the gas. The top Pt gate electrode was formed via shadow mask sputtering; thermal evaporation of Al formed the back side contact; the capacitance area of the formed Pt was approximately 4×10^{-4} cm^2, measured using an optical microscope. In addition, postmetallization annealing (PMA) was performed at 400 °C for one sample to evaluate the thermal stability of the fabricated $Pt/Al_2O_3/GaAs$ structures.

High-resolution transmission electron microscopy (HR-TEM) was used to characterize the variations in thickness of the deposited Al_2O_3 film after processing under the two different annealing environments. The structural composition and chemical bonding configuration were examined using, respectively, secondary ion mass spectrometry (SIMS) and x-ray photoelectron spectroscopy (XPS) with an Al Kα radiation source (1486.6 eV). To extract each chemical component from the photoemission spectra, a rigorous fitting process was adopted: after the peak positions had been ascertained, they were applied to reconstruct the original spectra and then to extract each respective contribution. During the deconvolution of the spectra, the peak areas were varied while maintaining the full width at half maximum and the ratio of the Gaussian to Lorentzian distribution constant. In addition, we measured the frequency-dependent capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics using an HP4284 *LCR* meter and a Keithley 4200 system, respectively, to determine the quality of the Al_2O_3–GaAs interface. The interface state density (D_{it}) was calculated using the conductance method[18] based on the measured conductance-voltage (*G-V*) curves.

III. RESULTS AND DISCUSSION

A. Effect of surface sulfidation

Figure 1 displays As $2p_{3/2}$ and Ga $2p_{3/2}$ photoemission spectra of the as-deposited $Al_2O_3/GaAs$ bilayer with and without $(NH_4)_2S$ interfacial passivation; the thickness of the overlying Al_2O_3 thin film after 60 deposition cycles was estimated to be approximately 63 (±3) Å. Thus, we employed the high surface sensitivity of this technique (maximum sampling depths of approximately 31 and 55 Å for the As $2p_{3/2}$ and Ga $2p_{3/2}$ spectra, respectively) to characterize the content of GaAs-related chemical species diffused into the high-*k* layer.[19] In accordance to the Ga $2p_{3/2}$, As $2p_{3/2}$, Al 2*p*, and O 1*s* core levels, we evaluated the average concentration of existing GaAs oxides and the stoichiometric ratio of O to Al, based on the mixture of Ga_2O_x and As_2O_x in the Al_2O_x bulk layer. As indicated in Table I, the concentrations of both the Ga and As oxide species were much less than 0.5%. So that, we infer that both kinds of native oxides, As_2O_x and Ga_2O_x, in the forms of their stoichiometric oxides and suboxides more likely formed close to oxide-substrate interface. But, we cannot rule out the possibility that a tiny amount of As oxides diffused into the Al_2O_3 high-*k* film during deposition at substrate temperature up to 300 °C. Besides, the formation of these oxides, in particular, the gallium oxides, could be suppressed by forming Ga- and As-related sulfur bonds at the dielectric interface. Interestingly, it appears that the stoichiometry of Al_2O_x in the deposited film may correlate with the degree of GaAs oxides formed nearby the interface. Provided that Al_2O_3 was directly deposited on GaAs, the O/Al chemical ratio was as high as 1.75, i.e., an oxygen-enriched Al_2O_x dielectric film; long-term sulfide immersion could return this value to a nearly ideal stoichiometric ratio of 1.57 as a result of the enhanced surface stability.

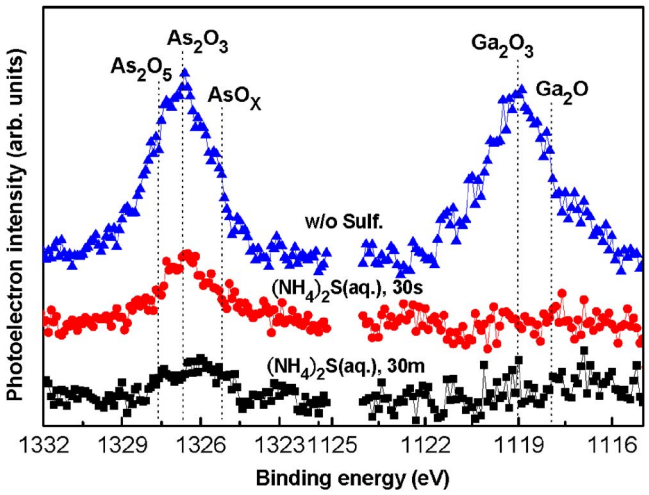

FIG. 1. (Color online) As $2p_{3/2}$ and Ga $2p_{3/2}$ XPS spectra of as-deposited ALD-Al_2O_3 thin films on GaAs substrates without and with $(NH_4)_2S$ sulfide passivation.

The As 3*d* and Ga 3*d* core level spectra in Fig. 2 allowed us to characterize the interfacial composition close to the substrate because the inelastic mean free paths were above 25 Å. We found that an amorphous As layer was present on

TABLE I. Calculated relative concentrations of GaAs oxides and stoichiometric O-to-Al ratios in as-deposited ALD-Al_2O_3 thin films before and after chemical treatment with $(NH_4)_2S$. Note that the As $2p_{3/2}$, Ga $2p_{3/2}$, Al 2*p*, and O 1*s* core levels were used by considering the atomic sensitivity factor.

	Ga (%)	As (%)	Al (%)	O (%)	O/Al ratio
Control (HCl/H_2O, 1:10)	0.2	0.2	36.3	63.3	1.75
$(NH_4)_2S_{aq}$ (2%, 30 s)	0	0.1	36.9	63.0	1.70
$(NH_4)_2S_{aq}$ (2%, 30 min)	0	0.05	38.8	61.15	1.57

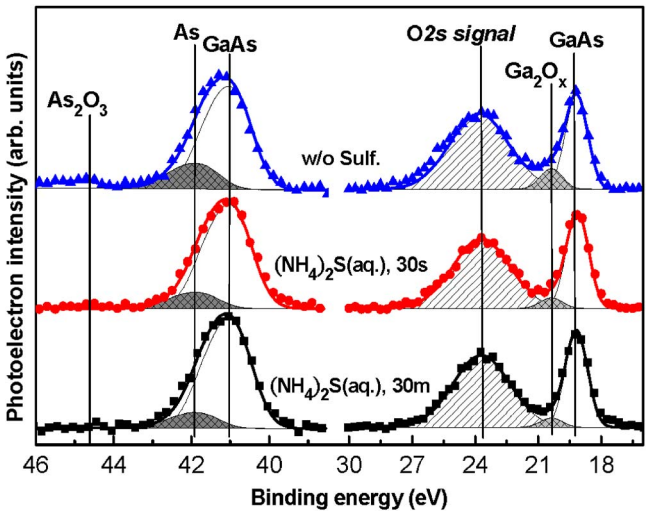

FIG. 2. (Color online) As 3*d* and Ga 3*d* XPS spectra of as-deposited ALD-Al_2O_3 thin films on GaAs substrates with and without $(NH_4)_2S$ sulfide passivation.

the bulk GaAs; moreover, its content could be decreased upon chemical treatment with $(NH_4)_2S$. We suggest that these interfacial As atoms could have arisen through two mechanisms: (a) the dilute HCl solution used to clean the GaAs might have led to the formation of elemental As atoms covering the GaAs surface;[20] (b) thermal transformation of the surface As oxides might have occurred through reactions with the GaAs substrate.[21] The As suboxides can desorb at approximately 150–200 °C, and the As_2O_x species having higher oxidization states ($x=3$ or 5) will sublime at temperatures of approximately 250–300 °C.[21–23] This ready thermal desorption indicates that mechanism (b) probably occurred during ALD deposition at 300 °C. We also calculated the relative contributions of elemental As and the As_2O_x and Ga_2O_x components in the respective As 3*d* and Ga 3*d* spectra (Table II). Evidently, the sulfur-terminated GaAs surface successfully decreased the content of the As-rich layer and its chemical oxides.

The O 2*s* photoelectron signal observed at 23.4 eV, which mostly originated from the overlying Al_2O_3 thin film, overlapped with the Ga 3*d* core level. The content of Ga–O oxide species existing near the Al_2O_3–GaAs interface decreased after sulfidization. According to the literature,[24,25] the Ga–S chemical bond, relative to the As–S bond, has the higher bond strength up to 400 °C, thereby effectively restraining the growth of Ga_2O_x. These sulfur species are not readily identified in a S 2*p* spectrum because of partial overlap with the signal of bulk Ga 3*s*, but a small number of GaS_x bonds were detectable at a peak position of approximately 162.2 eV (not shown here).[26] Along with the high stabilization of the Ga_2O_3 stoichiometric oxide, these features taken together reasonably explain the absence of the Ga–O signal in the Ga $2p_{3/2}$ spectra after surface sulfidization. In view of the improved behavior, we believe that the sulfur-terminated GaAs substrate enhanced the deposition quality and dielectric stoichiometry of the ALD-Al_2O_3 thin films.

TABLE II. Chemical bonding ratios of As 3*d* and Ga 3*d* core levels determined by fitting the XPS data from Fig. 2. Note that the contribution of the O 2*s* emission has been excluded.

	As 3*d* and Ga 3*d*		
	$As-As/As_{total}$ (%)	As_2O_x[a]$/As_{total}$ (%)	Ga_2O_x[b]$/Ga_{total}$ (%)
Control (HCl/H_2O, 1:10)	18.5	5	17.70
$(NH_4)_2S_{aq}$ (2%, 30 s)	13.4	0	9.84
$(NH_4)_2S_{aq}$ (2%, 30 min)	12.8	0	8.86

[a]The As_2O_x chemical species include As_2O_5, As_2O_3, and As suboxides.
[b]The Ga_2O_x chemical species include Ga_2O_3 and Ga suboxides.

Figure 3 displays the *C-V* and *I-V* characteristics of the various samples. The $(NH_4)_2S$-treated sample displayed a higher oxide capacitance accompanying a decreased *C-V* frequency dispersion, relative to those of the untreated sample; a reduction in hysteresis width and gate leakage current (J_g) were also achieved [Figs. 3(b) and 3(c)]. These results are indicative of the abatement of the Fermi level pinning effect in the capacitor properties; in other words, modulation of the surface potential and carrier manipulation was enhanced. As stated above, sulfide pretreatment suppressed the amounts of unstable As–As and As–O species, which are believed to be a source of high-density interfacial traps. The value of D_{it} close to the midgap was estimated to be approximately 1×10^{13} cm^{-2} eV^{-1} for the untreated sample; subsequent sulfide passivation reduced this value to approximately 7×10^{12} cm^{-2} eV^{-1}. Previous studies have found that sulfidized GaAs improved the MOS characteristics as a result of eliminating As-related surface defects.[27,28] The subsequent PMA at 400 °C, however, not only caused a larger frequency dispersion and broadened hysteresis width at the depletion region but also increased the value of J_g by nearly four orders of magnitude. The underlying mechanisms responsible for the PMA-induced gate leakage degradation are discussed below.

B. Effect of thermal annealing gas environment

To explore the degradation of the electrical characteristics that were due to N_2 annealing, we first compared HR-TEM images of the Pt/Al_2O_3 bilayers deposited on the sulfide-treated GaAs after PDA under N_2 and O_2 atmospheres [Figs. 4(a)–4(c)]. We did not observe the existence of the interfacial layer; the deposited Al_2O_3 also exhibited an amorphous phase after PDA at 600 °C. Most importantly, the O_2-processed sample revealed a bright Al_2O_3 thin film and an interface that was indistinct with respect to the upper Pt metal and GaAs substrate, whereas the N_2-processed sample revealed a relatively dark, thick Al_2O_3 film possessing a sharp interface. We believe that the O_2 used as the feed gas was effective in densifying the ALD-Al_2O_3 gate dielectric and repairing the inner bond imperfections, e.g., dangling bonds and oxygen vacancies. Meanwhile, a great degree of interdiffusion occurred at the dielectric-substrate interface, which can be attributed to the relatively high probability of oxygen diffusing into the GaAs substrate,[29] resulting in the blurred interface for the O_2-processed system.

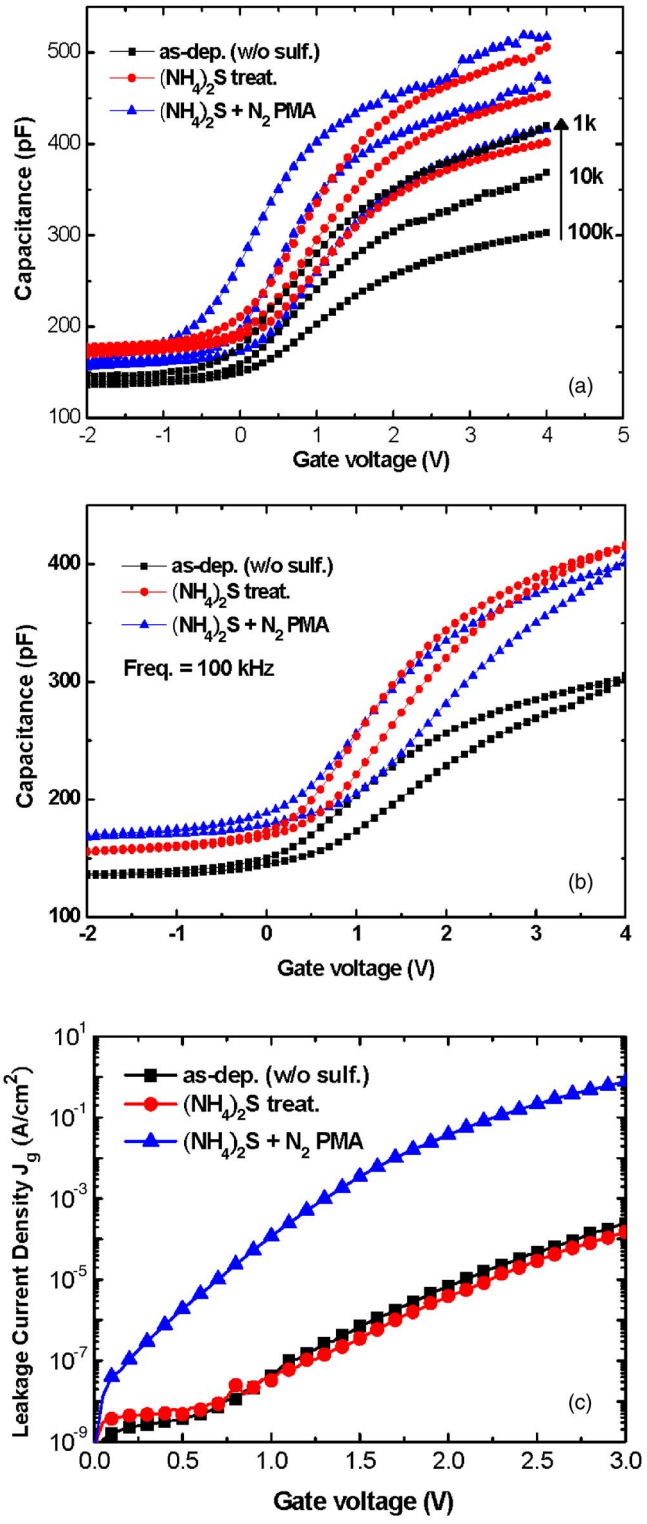

FIG. 3. (Color online) (a) Multifrequency and (b) bidirectional *C-V* characteristics and (c) gate leakage current (*I-V*) curves of GaAs MOS capacitors with as-deposited Al_2O_3 thin films after $(NH_4)_2S$ passivation and PMA at 400 °C.

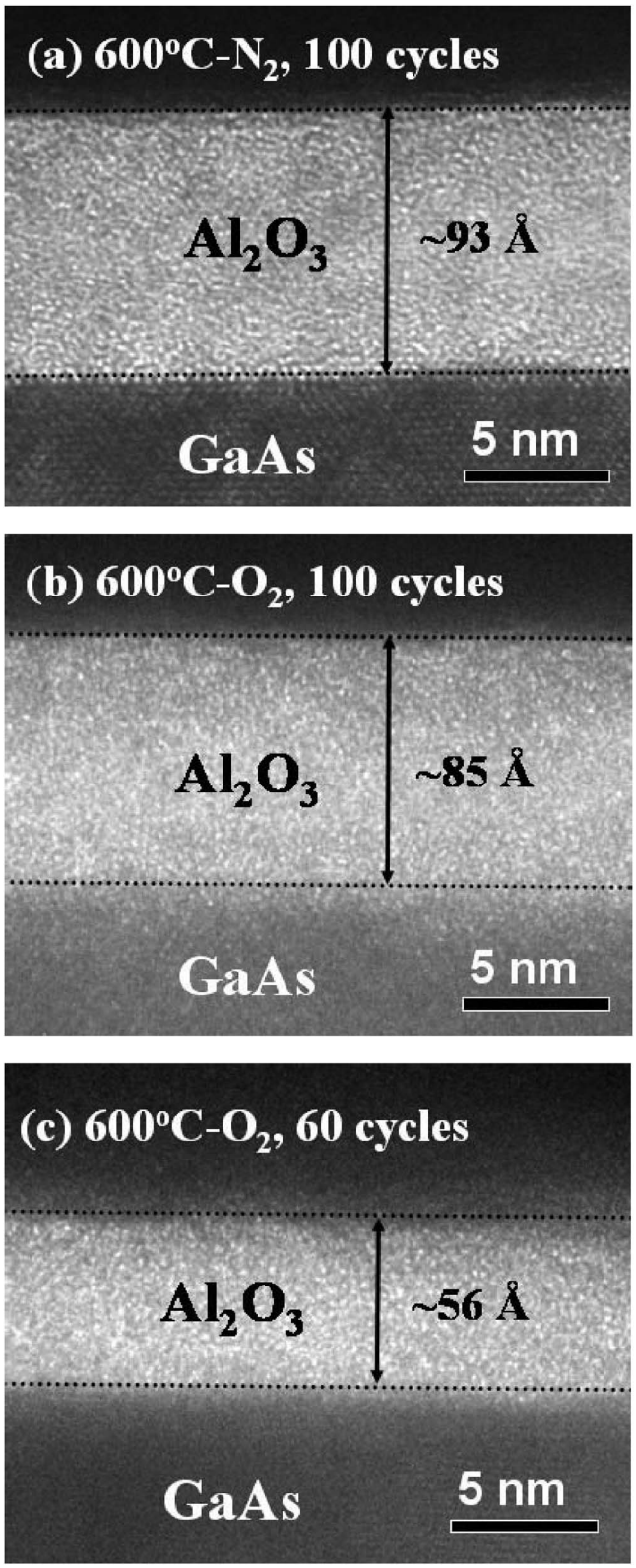

FIG. 4. HRTEM images of Pt/Al_2O_3/sulfidized-GaAs structures with different deposition cycles and PDA conditions: (a) 100 cycles, N_2 PDA; (b) 100 cycles, O_2 PDA; (c) 60 cycles, O_2 PDA. PDA temperature: 600 °C.

Next we examined the impact of thermal annealing on the multifrequency *C-V* curves, as illustrated in Figs. 5(a) and 5(b); each inset displays the *C-V* hysteresis width measured at 100 kHz. For both deposition conditions, the O_2-annealed samples exhibited higher oxide capacitance and decreased hysteresis phenomena with respect to the N_2-annealed samples; we attribute this finding mainly to the highly improved dielectric quality and the thinner film thickness. We also found that electron trapping was responsible for the clockwise hysteresis loop,[17] where the hysteresis widths after O_2 and N_2 PDA were approximately 0.3 and

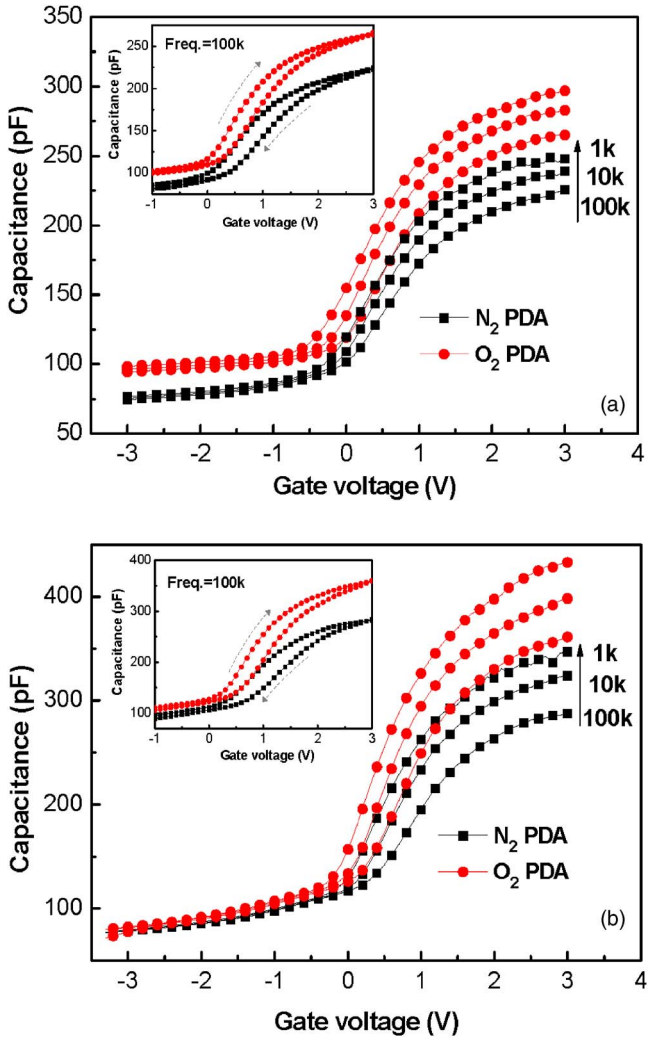

FIG. 5. (Color online) Multi-frequency *C-V* curves of sulfidized-GaAs MOS capacitors with Al_2O_3 thin films annealed for (a) 100 and (b) 60 deposition cycles. Each inset displays the respective *C-V* hysteresis measured at 100 kHz.

0.4 V, respectively. This situation reflected the smaller density of slow traps that resided around the dielectric interface after performing O_2 annealing. In contrast, the *I-V* characteristics in Fig. 6 are remarkably different: N_2 PDA severely deteriorated the J_g characteristics, as in the PMA case in Fig. 3(c), whereas the O_2 ambient alleviated the degradation phenomenon. From a plot of the value of J_g (at V_g=2 V) versus the capacitance-equivalent thickness (CET), the value of J_g at a CET of 40 Å was reduced by nearly three orders of magnitude after replacing N_2 with O_2 as the annealing gas (inset to Fig. 6). We ascribe the dramatically increased value of J_g to one or both of the following mechanisms: (a) the elemental As overlayer that acted as a metallic contamination source nearby the oxide-bulk interface increased the surface recombination velocity, with fast diffusion resulting in poor insulator properties; (b) high-temperature processing caused the generation of surface pits or holes within the GaAs substrate, thus increasing the surface roughness.[21] Excess As atoms might have been produced during either the decomposition of GaAs itself or the chemical transformation of oxide species through reactions with the bulk GaAs; meanwhile,

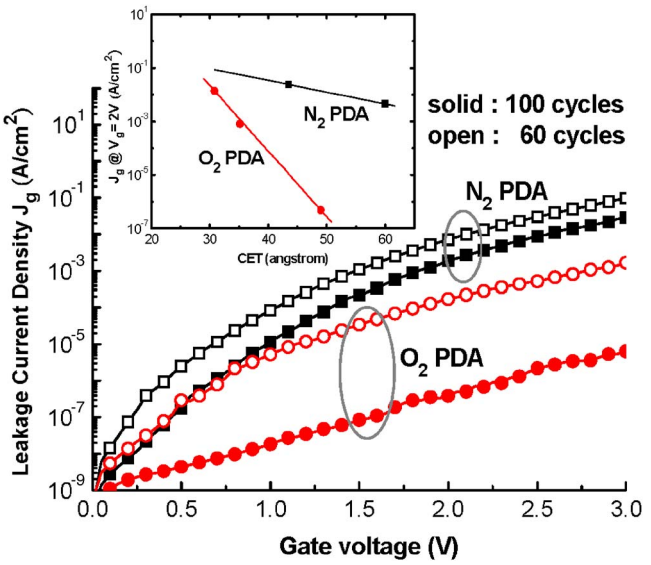

FIG. 6. (Color online) *I-V* Characteristics of the MOS capacitors analyzed in Fig. 5. Inset: Plot of J_g (at V_g=2 V) vs CET.

the inhomogeneous voids formed also deteriorated the surface morphology. We expected a relatively low density of formed voids after annealing because of the coverage of an amorphous Al_2O_3 film on GaAs substrate. Thus, we inferred that the N_2-annealed Al_2O_3/GaAs structures suffered from relatively severe desorption and transformation of the As_2O_x and Ga_2O_x mixed oxides; in addition, more As atoms were segregated at the interface. In light of this behavior, we would expect degradation of the gate leakage characteristics to be accelerated after N_2 annealing. To support our hypothesis, we performed a dielectric reliability test (Fig. 7) with regard to this degradation behavior. The Pt/ALD-Al_2O_3/GaAs capacitors were stressed under the constant voltage stress (V_g) of 5 V and a constant oxide electrical field (E_{ox}) of 8.5 MV cm^{-1}. Irrespective of the dielectric stress method employed, we found that the sulfidization procedure improved the dielectric reliability. The sulfidized sample that underwent subsequent O_2 annealing possessed

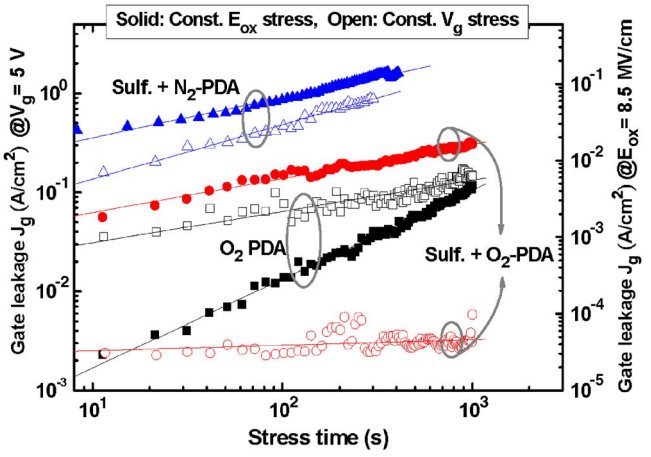

FIG. 7. (Color online) Stress time dependence of the gate leakage J_g for Pt/ALD-Al_2O_3/GaAs MOS capacitors under a constant V_g stress of 5 V (at the left *y*-axis) and a constant E_{ox} stress of 8.5 MV cm^{-1} (at the right *y*-axis), respectively.

TABLE III. Solid state chemical reactions of Ga–As–O associated systems. All these equations are separated into four parts.

	T_c (°C)	ΔG_f (kJ mol^{-1})
(A) Transformation reactions[a]		
(I) $4AsO_x(s) \rightarrow 4As(s)$ or $As_4(g)\uparrow + xO_2(g)$	150–200	···
(II) $As_2O_3(s)+2GaAs(s) \rightarrow Ga_2O_3(s)+4As(s)$ or $As_4(g)\uparrow$	290–350	−280/−225 (at 300 K) and −277/−233 (at 600 K)
(III) $As_2O_3(s)+4Ga(s,l) \rightarrow Ga_2O_3(s)+2GaAs(s)$	···	−564 (at 300 K) and −521 (at 600 K)
(IV) $As_2O_3(s)+2Ga(s,l) \rightarrow Ga_2O_3(s)+2As(s)$ or $As_2(g)\uparrow$	···	−422/−347 (at 300 K) and −399/−403 (at 600 K)
(V) $Ga(s,l)+As(s) \rightarrow GaAs(s)$	···	−70 (at 300 K) and −50 (at 900 K)
(B) Oxidation reactions[b]		
(I) $2GaAs(s)+3/2O_2(g) \rightarrow As_2O_3(s)+2Ga(s,l)$	···	−435 (at 300 K) and −376 (at 600 K)
(II) $2Ga(s,l)+3/2O_2(g) \rightarrow Ga_2O_3(s)$	···	−999 (at 300 K) and −896 (at 600 K)
(III) $2As(s)+3/2O_2(g) \rightarrow As_2O_3(s)$	···	−576 (at 300 K) and −497 (at 600 K)
(IV) $As_2O_3(s)+O_2(g) \rightarrow As_2O_5(s)$	···	−207 (at 300 K) and −141 (at 600 K)
(C) GaAs decomposition/As vaporization reactions (inhibited at room temperature)[c]		
(I) $2As(s) \rightarrow As_2(g)$	300	139 (at 300 K) and 48 (at 875 K)
(II) $4As(s) \rightarrow As_4(g)$	300	76 (at 300 K) and −81 (at 875 K)
(III) $4GaAs(s) \rightarrow 4Ga(s,l)+4As(s)$ or $As_4(g)\uparrow$	500–600	280/379 (at 300 K) and 200/195 (at 900 K)
(D) Ga_2O[d] formation reactions (inhibited at room temperature)[e]		
(I) $As_2O_3(s)+6GaAs(s) \rightarrow 3Ga_2O(s)+8As(s)$ or $2As_4(g)\uparrow$	···	6/202 (at 300 K) and $\ll$6 (at 600 K)
(II) $Ga_2O_3(s)+4Ga(s,l) \rightarrow 3Ga_2O(s)$	500–600	7 (at 300 K) and $\ll$7 (at 900 K)
(III) $Ga_2O_3(s)+4GaAs(s) \rightarrow 3Ga_2O(s)+4As(s)$ or $As_4(g)\uparrow$	400–500	287/385 (at 300 K) and $\ll$287 (at 900 K)

[a]References 22, 23, and 37.
[b]Reference 38.
[c]References 23 and 33.
[d]The standard molar Gibbs free energy of formation (ΔG_f) for Ga_2O(s) was assumed to be −330 kJ mol^{-1}, based on the standard molar enthalpy of formation (ΔH_f) of −356 kJ mol^{-1} at 300 K (Ref. 32).
[e]References 23, 35, and 37.

superior dielectric reliability, relative to that which underwent N_2 annealing, in accordance to the slower rate of increase in the value of J_g. These findings indicate that the annealing environment is a crucial factor in determining the electrical performance of high-k/GaAs structures. The degraded quality of the N_2-annealed sample with respect to the O_2-annealed one shall be closely linked to severe As_2O_x desorption and the extent is not so drastic to cause the increase of the interface roughness. This is because a relatively low temperature of 600 °C annealing was employed as compared to the previous observation reported by Passlack *et al.* that the Ga_2O_3/GaAs interface is very smooth after annealing below 700 °C and severely degrades with 780 °C annealing.[16]

Table III provides a comprehensive list of the accessible solid state reactions involved in the Ga–As–O phase diagram[30,31] to aid us in determining the transformation phenomena that occurred during annealing. The critical temperature T_c is defined as the temperature at which the reaction becomes thermodynamically favorable, i.e., where the Gibbs free energy of formation (ΔG_f) is less than zero; we obtained the values of T_c from experimental results reported in the literatures.[21–23,34] We also calculated the value of ΔG_f for each of these stoichiometric equations.[32,33] If ΔG_f is greater than zero, the chemical reaction will not proceed; for example, the mechanisms associated with Ga_2O formation are inhibited at room temperature, but an increase in temperature enhances the driving kinetics of the reaction. Because various kinds of GaAs chemical products desorb and/or transform during high-temperature processing, we performed XPS and SIMS analyses to better characterize the electrical differences.

The As $2p_{3/2}$ and Ga $2p_{3/2}$ spectra in Fig. 8 indicate that the diffusion of GaAs chemical species was enhanced within the Al_2O_3 gate dielectric after thermal annealing; we extracted the contribution of each chemical component. In the following discussion we denote the N_2-annealed capacitor that underwent sulfide treatment as the "SN sample" and denote the O_2-annealed capacitors without and with sulfide treatment as the "O sample" and "SO sample," respectively. The As $2p_{3/2}$ spectra revealed an increased incorporation of arsenic oxides, including As_2O_5, As_2O_3, and AsO_x, relative to their content in the as-deposited Al_2O_3 film. We observed similar behavior in the Ga $2p_{3/2}$ spectra: both the Ga_2O_3 and GaO_x oxides were slightly enriched after annealing, with the SN sample having relative higher concentrations. From the atomic quantification, Table IV indicates that the amount of diffused arsenic oxides was larger, by about one order of

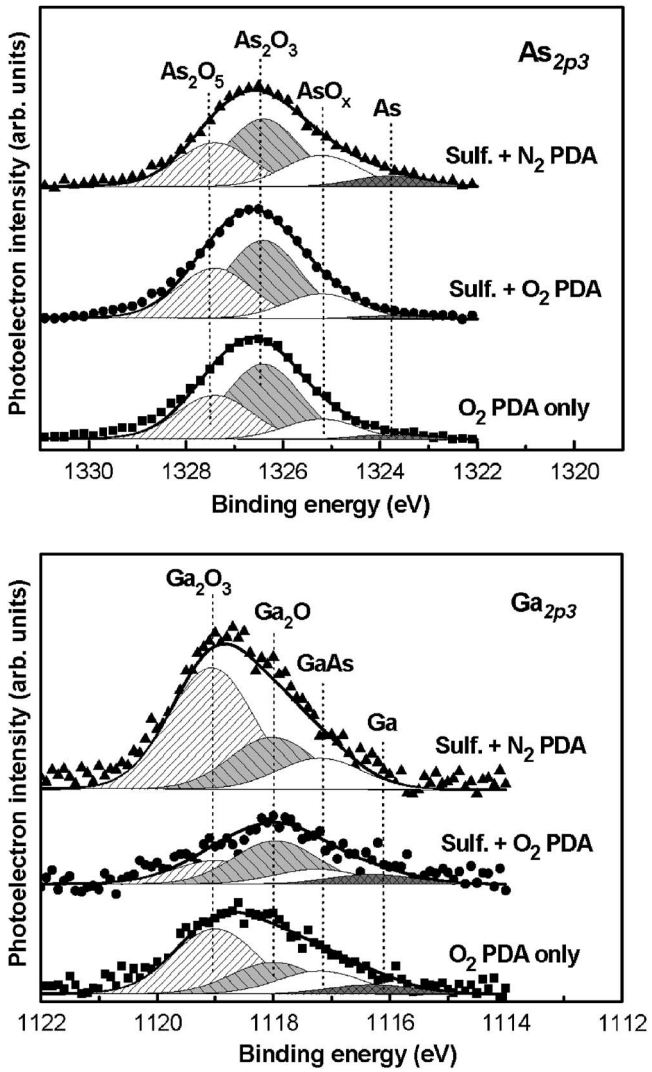

FIG. 8. As $2p_{3/2}$ and Ga $2p_{3/2}$ XPS spectra of 600 °C-annealed Al_2O_3 thin films on the sulfidized GaAs substrate. The contributing chemical components were extracted and are displayed in the respective spectra.

magnitude, than that of the gallium oxides in the annealed Al_2O_3; this behavior is similar to that of the oxide layer formed during thermal oxidation of a GaAs surface.[36] In addition, only the O sample after annealing at 600 °C presented an oxygen-enriched Al_2O_x film; we attribute this finding to a portion of the sulfur atoms filling a number of vacancies inside the high-*k* gate dielectric, thereby avoiding overoxidization in the sulfidized samples during PDA.

Table III-(A) indicates that the value of T_c for the desorption of arsenic oxides ranges from 150 to 350 °C; these transformations are thermodynamically favorable at room temperature. In contrast, the higher thermal stability of the Ga-based oxide compounds inhibits the reduction of nonvolatile Ga_2O_3 into Ga_2O [Table III-(D)]; consequently, its value of T_c is higher (400–600 °C). Because of the low sublimation point of the oxides of arsenic, volatile As_2O_3 oxide first reacts with either the GaAs substrate or interstitial Ga atoms to form a Ga_2O_3 layer and segregated As close to the interface. It is possible that the highly stable Ga_2O_3 oxide also reacts with the substrate again to produce nonstoichiometric Ga_2O along with the As coproducts under high-temperature annealing at 600 °C. Most of these As species—in the form of elemental As and/or gaseous As_4—are oxidized during the desorption event and then trapped inside the dielectric film. Note that Ga_2O_3 formation can arise through several transformation paths; for example: $As_2O_3+2GaAs \rightarrow Ga_2O_3+4As$ or As_4. Because the O_2 environment provides additional reaction paths [Table III-(B)], the content of chemical products is likely to be somewhat different to that in the N_2 annealing case. This situation can be explained in terms of the chemical reaction principle that kinetics naturally drive several oxidation mechanisms—e.g., the oxidation of GaAs, As, and As_4—resulting in a deceleration of the rate of transformation of As_2O_x compounds as well as the generation of As defects in the O_2 ambient.[38] In addition, even if molecular oxygen prefers to react with Ga atoms over As atoms, the As species will still have a higher probability of oxidation because they are more readily desorbed.[39] When the content of arsenic oxides increases in the upper area of the dielectric film they can act as a block, which in turn hinders the diffusion of oxygen into the dielectric-substrate region. These phenomena result in our observation of an enriched amount of As_2O_x with a low Ga_2O_x concentration for both the SO and O samples, a finding that is opposite to the behavior of the SN sample. Another interesting phenomenon visible in the $2p_{3/2}$ spectra is that PDA under N_2 resulted in the formation of some metallic As, whereas some elemental Ga appeared after PDA under O_2. This finding provides direct evidence of the fast generation of As species in the N_2 ambient. On the other hand, as far as the source of these Ga atoms is concerned, we speculate that the oxidation of the Al_2O_3/GaAs interface and decomposition of the GaAs substrate are responsible for the supply of free Ga atoms.[23,38] It should be pointed out that as regarding the reactions related to Al and these indiffused Ga or As oxides, most possible reaction we presume is the reaction of Al_2O_3 with Ga_2O_3 due to the higher thermal stability relative to As_2O_3. However, in our study the highest RTA temperature is 600 °C, probably not enough to make Al react with Ga oxides;[40] these thermal processes are excluded here and still need further investigation.

TABLE IV. Calculated relative concentration of GaAs oxides and stoichiometric O-to-Al ratios in the N_2- and O_2-annealed ALD-Al_2O_3 thin films with and without $(NH_4)_2S$ surface passivation.

	Ga (%)	As (%)	Al (%)	O (%)	O/Al ratio
Sulfide+N_2 600 °C PDA	0.3	2.0	34.8	62.9	1.80
Sulfide+O_2 600 °C PDA	0.11	2.94	35.1	61.8	1.76
O_2 600 °C PDA only	0.24	3.87	30.0	65.8	2.19

Figure 9 presents the highly bulk-sensitive As 3*d* and Ga 3*d* photoemissions; Table V provides the chemical bonding ratio of the contributed chemical components for convenient characterization. We observe that annealing at 600 °C further decreased the percentage of interfacial As presented in the overall As 3*d* spectra, with respect to that in the as-deposited Al_2O_3/GaAs structures (Fig. 2, Table II). Even though the desorption event contributed to the formation of either As or As_4, most of the As atoms escaped into the

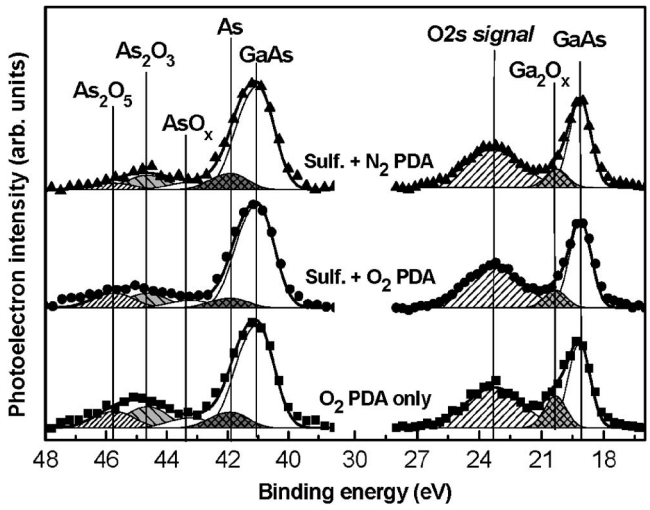

FIG. 9. As 3*d* and Ga 3*d* XPS spectra of 600 °C-annealed Al_2O_3 thin films on the sulfidized GaAs substrate. The contributed chemical components were extracted and are displayed in the respective spectra.

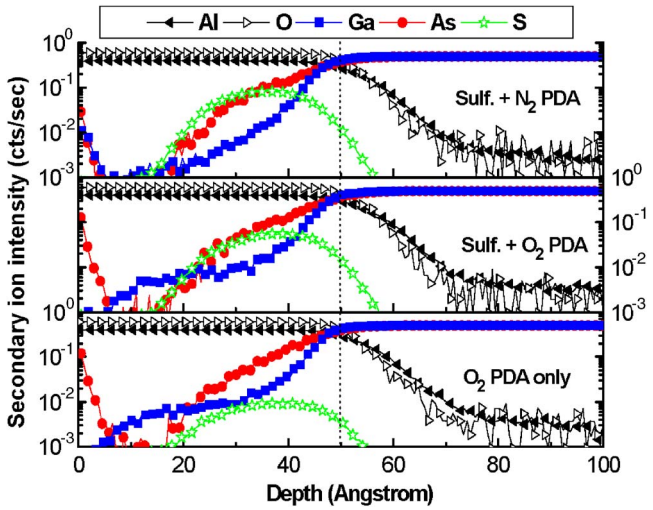

FIG. 10. (Color online) SIMS depth profiles of the Al_2O_3/GaAs samples analyzed in Fig. 9. The diffusion of As- and Ga-related chemical species into overlying high-*k* film was observed.

atmosphere or were further oxidized into various oxidation states. A substantial amount of Ga_2O_x oxides was generated accordingly through chemical transformation. We also observed that the additional sulfide pretreatment of the SO sample made it (relative to the O sample) more highly resistant to the growth of these undesirable components. Figure 10 illustrates the respective SIMS depth profiles; the thickness of the Al_2O_3 thin film, which was deposited at 300 °C for 50 cycles, was approximately 50 (±3) Å after PDA at 600 °C. Of primary interest is the distribution of the As, Ga, and S species in the overlying Al_2O_3 high-*k* film. We found that a higher concentration of As was presented around the bottom of the Al_2O_3 bulk film, coinciding with the diffusion of As-enriched oxides and the interfacial arsenic layer. Another feature is the observation of a small tails of Ga species at a depth of approximately 10–30 Å for the SO and O samples only, probably related to a trace of outdiffused Ga elements, the detailed mechanism of which requires further investigation. On the other hand, the S signal detected in the O sample was due to mass interference of molecular oxygen in the SIMS analysis of the oxide film. We believe that the S atoms did exist even after high-temperature processing, as determined after subtracting the induced signal of the mass interference used as the baseline background. The corresponding XPS analysis in Table IV indicates that the sulfidized samples were relatively less oxygen excessive (Al/O ratio=1.78) with respect to the HCl-last sample (Al/O ratio=2.2). Meanwhile, the smaller *C-V* hysteresis width after sulfidization is indicative of less charge trapping in the Al_2O_3 dielectric (not shown here). Thus, we conclude that most of the S atoms diffused into the high-*k* film and probably occupied either the vacancy sites or pre-existing defects; as a result, this process facilitated the improvement in the quality of the Al_2O_3 gate dielectrics as well as their electrical performance.

TABLE V. Chemical bonding ratios of As 3*d* and Ga 3*d* core levels determined by fitting the XPS data from Fig. 9. Note that the contribution of the O 2*s* emission has been excluded.

	As 3*d* and Ga 3*d*		
	$As-As/As_{total}$ (%)	As_2O_x[a] $/As_{total}$ (%)	Ga_2O_x[b] $/Ga_{total}$ (%)
Sulfide+N_2 PDA at 600 °C	10.6	20.6	17.4
Sulfide+O_2 PDA at 600 °C	6.2	26.0	16.8
O_2 PDA at 600 °C only	9.2	30.8	27.6

[a]The As_2O_x chemical species include As_2O_5, As_2O_3, and As suboxides.
[b]The Ga_2O_x chemical species include Ga_2O_3 and Ga suboxides.

IV. CONCLUSIONS

In this study, we systematically examined the interfacial characteristics and MOS properties of ALD-Al_2O_3 dielectric films deposited on sulfidized GaAs substrates. The sulfidation pretreatment diminished the formation of GaAs native oxides and elemental As coverage close to dielectric interface, thus improving the effect of Fermi level pinning on the Al_2O_3/Ge capacitors. The sulfidized samples displayed not only smaller frequency dispersions with higher oxide capacitances but also decreased hysteresis widths, interfacial state densities, and gate leakages (J_g). In addition, a nearly stoichiometric Al_2O_3 high-*k* film exhibiting higher resistivity to dielectric overoxidation was obtained after performing sulfidization. The nature of the thermal annealing environment also affected several characteristics of the systems; for example, the use of an O_2 ambient, relative to N_2, further densified the Al_2O_3 dielectric film, alleviated charge trapping, and decreased the amount of metallic As generated, thereby improving the reliability of the value of J_g. We have clarified these phenomena in terms of identifying the underlying thermochemical mechanisms.

ACKNOWLEDGMENTS

This study was sponsored mainly by the National Science Council of the Republic of China under Contract No. NSC94-2215-E009-066.

[1]S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, Tech. Dig. - Int. Electron Devices Meet. **2005**, 763.
[2]M. H. Zhang, I. J. Ok, H. S. Kim, F. Zhu, T. Lee, G. Thareja, L. Yu, and J. C. Lee, Appl. Phys. Lett. **89**, 042902 (2006).
[3]J. Reed, Z. Fan, G. B. Gao, A. Botchkarev, and H. Morkoc, Appl. Phys. Lett. **64**, 2706 (1994).
[4]H.-L. Lu, L. Sun, S.-J. Ding, M. Xu, D. W. Zhang, and L.-K. Wang, Appl. Phys. Lett. **89**, 152910 (2006).
[5]C. P. Chen, Y. J. Lee, Y. C. Chang, Z. K. Yang, M. Hong, J. Kwo, H. Y. Lee, and T. S. Lay, J. Appl. Phys. **100**, 104502 (2006).
[6]M. Zhu, C.-H. Tung, and Y.-C. Yeo, Appl. Phys. Lett. **89**, 202903 (2006).
[7]S. Arabasz, E. Bergignat, G. Hollinger, and J. Szuber, Vacuum **80**, 888 (2006).
[8]V. N. Bessolov, E. V. Konenkova, and M. V. Lebedev, J. Vac. Sci. Technol. B **14**, 2761 (1996).
[9]Y. Dong, X. M. Ding, X. Y. Hou, Y. Li, and X. B. Li, Appl. Phys. Lett. **77**, 3839 (2000).
[10]D. S. L. Mui, D. Biswas, J. Reed, A. L. Demirel, S. Strite, and H. Morkoc, Appl. Phys. Lett. **60**, 2511 (1992).
[11]Z. Chen and D. Gong, J. Appl. Phys. **90**, 4205 (2001).
[12]D. Shahrjerdi, M. M. Oye, A. L. Holmes, Jr., and S. K. Banerjee, Appl. Phys. Lett. **89**, 043501 (2006).
[13]M. H. Zhang, I. J. Ok, H. S. Kim, F. Zhu, T. Lee, G. Thareja, L. Yu, and J. C. Lee, Appl. Phys. Lett. **89**, 042902 (2006).
[14]A. Jaouad, V. Aimez, C. Aktik, K. Bellatreche, and A. Souifi, J. Vac. Sci. Technol. A **22**, 1027 (2004).
[15]M.-K. Lee, C.-F. Yen, J.-J. Huang, and S.-H. Lin, J. Electrochem. Soc. **153**, F266 (2006).
[16]M. Passlack, J. K. Abrokwah, Z. Yu, R. Droopad, C. Overgaard, and H. Kawayoshi, Appl. Phys. Lett. **82**, 1691 (2003).
[17]M. H. Zhang, M. Oye, B. Cobb, F. Zhu, H. S. Kim, I. J. Ok, J. Hurst, S. Lewis, A. Holmes, J. C. Lee, S. Koveshnikov, W. Tsai, M. Yakimov, V. Torkanov, and S. Oktyabrsky, J. Appl. Phys. **101**, 034103 (2007).
[18]W. A. Hill and C. C. Coleman, Solid-State Electron. **23**, 987 (1980).
[19]NIST Electron Inelastic-Mean-Free-Path Database 71 (v. 1.1), National Institute of Standards and Technology, 2000.
[20]K. W. Frese and S. R. Morrison, Appl. Surf. Sci. **8**, 266 (1981).
[21]A. G. Cervantes, Z. R. Alvarez, M. L. Lopez, E. L. Luna, and I. H. Calderon, Thin Solid Films **373**, 159 (2000).
[22]J. P. Contour, J. Massies, H. Fronius, and K. Ploog, Jpn. J. Appl. Phys., Part 2 **27**, L167 (1988).
[23]M. Yamada and Y. Ide, Surf. Sci. **339**, L914 (1995).
[24]H. Sugahara, M. Oshima, H. Oigawa, H. Shigekawa, and Y. Nannichi, J. Appl. Phys. **69**, 4349 (1991).
[25]H. Sik, Y. Feurprier, C. Cardinaud, G. Turban, and A. Scavennec, J. Electrochem. Soc. **144**, 2106 (1997).
[26]M. V. Lebedev, T. Mayer, and W. Jaegermann, Surf. Sci. **547**, 171 (2003).
[27]J.-K. Yang, M.-G. Kang, and H.-H. Park, J. Appl. Phys. **96**, 4811 (2004).
[28]L. J. Huang, W. M. Lau, S. Ingrey, D. Landheer, and J.-P. Noel, J. Appl. Phys. **76**, 8192 (1994).
[29]B. R. Chakraborty, N. Dilawar, S. Pal, and D. N. Bose, Thin Solid Films **411**, 240 (2002).
[30]Yu. V. Medvedev, Appl. Phys. Lett. **64**, 3458 (1994).
[31]C. D. Thurmond, G. P. Schwartz, G. W. Kammlott, and B. Schwartz, J. Electrochem. Soc. **127**, 1366 (2006).
[32]D. R. Lide, *CRC Handbook of Chemistry and Physics: a Ready-Reference Book of Chemical and Physical Data*, 84th ed. (CRC, Boca Raton, FL, 2003).
[33]O. Knacke, O. Kubaschewski, and K. Hesselmann, *Thermochemical Properties of Inorganic Substances* (Springer, Berlin, 1991).
[34]K. Tone, M. Yamada, Y. Ide, and Y. Katayama, Jpn. J. Appl. Phys., Part 2 **31**, L721 (1992).
[35]G. W. Smith, A. J. Pidduck, C. R. Whitehouse, J. L. Glasper, and A. M. Keir, Appl. Phys. Lett. **64**, 3458 (1994).
[36]S. C. Ghosh, M. C. Biesinger, R. R. LaPierre, and P. Kruse, J. Appl. Phys. **101**, 114322 (2007).
[37]S. C. Ghosh, M. C. Biesinger, R. R. LaPierre, and P. Kruse, J. Appl. Phys. **101**, 114321 (2007).
[38]D. A. Allwood, S. Cox, N. J. Mason, R. Palmer, R. Young, and P. J. Walker, Thin Solid Films **412**, 76 (2002).
[39]J. S. Song, Y. C. Choi, S. H. Seo, D. C. Oh, M. W. Cho, T. Yao, and M. H. Oh, J. Cryst. Growth **264**, 98 (2004).
[40]M. Takahashi, T. Nakatani, S. Iwamoto, T. Watanabe, and M. Inoue, J. Phys.: Condens. Matter **18**, 5745 (2006).