

Performance enhancement of excimer laser crystallized poly-Si thin film transistors with fluorine implantation technology

Chun-Hao Tu^a, Ting-Chang Chang^{b,*}, Po-Tsun Liu^c, Che-Yu Yang^a, Li-Wei Feng^a,
Yung-Chun Wu^d, Simon M. Sze^a, Chun-Yen Chang^a

^a Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan, ROC

^b Department of Physics and Institute of Electro-Optical Engineering, Center for Nanoscience and Nanotechnology, National Sun Yat-sen University, Taiwan, ROC

^c Department of Photonics and Display Institute, National Chiao Tung University, Hsin-Chu, Taiwan, ROC

^d Department of Engineering and System Science, National Tsing-Hua University, Hsinchu, Taiwan, ROC

Received 1 August 2006; received in revised form 18 July 2007; accepted 8 August 2007

Available online 16 August 2007

Abstract

Polycrystalline silicon thin film transistors (poly-Si TFTs) with the ion implantation of fluorine elements were investigated in this study. The electrical performance and reliability were reported comprehensively. Experimental work has shown the electrical characteristics of excimer laser crystallized F-ions-implanted poly-Si TFTs are improved effectively, especially for field effect mobility. It is also found that the fluorine piled up at the poly-Si interface during thermal annealing, for the TFT fabricated without a prior deposition of pad oxide. The stronger Si–F bonds replace the Si–Si/Si–H, leading to the superior electrical reliability. However, the dose of F ions is critical in poly-Si, or the electrical characteristics of TFT devices will be degraded.

© 2007 Published by Elsevier B.V.

Keywords: Poly-Si TFTs; Fluorine; Excimer laser crystallization

1. Introduction

In recent years the poly-Si TFTs were widely used in many applications, especially for active matrix liquid phase crystal displays (AMLCDs) [1,2]. The major advantage of the poly-Si TFTs for AMLCDs is in the significantly increased carrier mobility, as well as the ability to integrate the pixel switching elements, panel array, and peripheral driving circuit on the same substrates [3–5]. Low-temperature technology is required to realize commercial flat-panel displays on inexpensive glass substrate when manufacturing high performance poly-Si TFTs, since the maximum process temperature is restricted less than 600 °C. However, poly-Si TFTs suffer from undesirable leakage current from grain boundaries of polycrystalline silicon. Therefore, the methods, such as enlarging the grain size or passivating the defects, have been proposed to resolve the

detrimental effects [6–8]. Experimental results indicate that excimer laser annealing crystallizes amorphous silicon (a-Si) film to fabricate low temperature poly-Si TFTs with few in-grain defects [6,7]. For the excimer laser crystallization (ELC) process, the difference of thermal expansion coefficient between the molten poly-Si film and buffer oxide causes serious mechanical stress [8]. The mechanical stress is well known to cause numerous interface states and degrade the electrical properties of metal–oxide–semiconductors devices [9,10]. Moreover, the trap states present between the interface of poly-Si and buffer oxide were reported to degrade the electrical properties, such as on current (I_{ON}), subthreshold swings (S.S), and off current (I_{OFF}). It is believed that the reduction of trap states between poly-Si and buffer oxide improves the performance of poly-Si TFTs [8]. Based on this issue, trap state density elimination technology is also adopted to enhance the electrical properties. Hydrogen plasma treatment is a widely used method for passivating the trap states to avoid current leakage [11]. However, it is difficult to precisely control the

* Corresponding author.

E-mail address: tcchang@mail.phys.nsysu.edu.tw (T.-C. Chang).

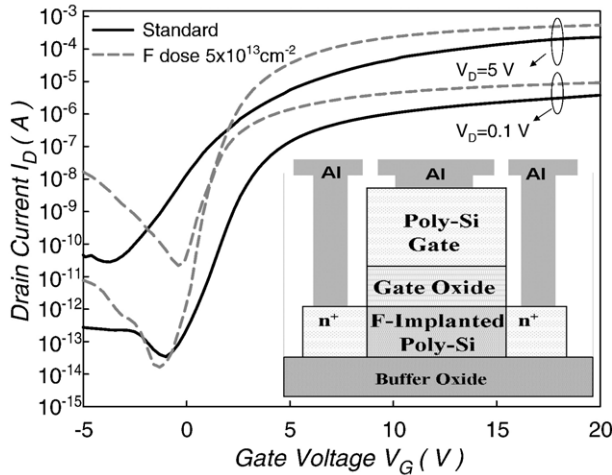


Fig. 1. The transfer characteristics of the poly-Si TFTs with F ions implantation dosage of $5 \times 10^{13} \text{ cm}^{-2}$, compared to the typically fabricated poly-Si TFTs (marked as Standard). (Insert is the schematic cross-section of the F-ions-implanted poly-Si TFT structure.)

concentration of hydrogen in the TFTs by the plasma treatment. F-ion implantation has recently been applied to improve the electrical characteristics of poly-Si films by eliminating defects at the grain boundaries [12,13]. The objective of F-ion implantation is to passivate undesirable strain bonds at the interface between poly-Si and SiO_2 and on the poly-Si surface. It has been found that the piling up of F at the interface between the poly-Si and the oxide can effectively reduce the strain bonds. However, the prior art required an extra oxide layer deposition and additional thermal annealing process. The extra process steps increase the difficulty for fabricating poly-Si TFTs. It is clearly indicated that the surface-oxidized a-Si also cause the F segregated to the poly-Si interface during thermal crystallization in our reported research [14,15]. Since the segregation of fluorine at the poly-Si and buffer oxide interface eliminates the mechanical stress, the release of mechanical strain and the trap state passivation can be performed using the ease F-ion implantation. Additionally, strong Si–F bonds replace the weaker Si–H and Si–Si bonds, enhancing the electrical DC stress reliability, compared to standard poly-Si TFTs.

This work will investigate the behaviors of fluorine in the poly-Si film after thermal annealing and the electrical characteristics of F-ions-implanted poly-Si TFTs. The various doses of F ions were implanted into the a-Si layer which was deposited first by low pressure chemical vapor deposition (LPCVD) system. Then, the re-crystallization was performed by using excimer laser annealing system.

2. Devices structure and fabrication

The 50-nm-thick undoped a-Si layer was deposited on oxide-coated silicon wafer by LPCVD system. The thickness of coated oxide is 550 nm. Then the F ions were implanted to the a-Si layer without any prior deposition of pad oxide. The ions implantation conditions were set at ion accelerating energy is

Table 1

The key electrical parameters of F-implanted poly-Si TFTs with ion dosage of $5 \times 10^{13} \text{ cm}^{-2}$, compared to the standard poly-Si TFT

| | $\mu_{FE} (\text{cm}^2/\text{V s})$ | $V_{TH} (\text{V})$ | s.s (V/dec) | Nt (10^{12} cm^{-2}) |
|--------------------------------------|-------------------------------------|---------------------|-------------|----------------------------------|
| STD | 56.7 | 3.07 | 0.61 | 5.18 |
| $F 5 \times 10^{13} \text{ cm}^{-2}$ | 103.9 | 1.19 | 0.30 | 3.07 |

11 keV and the doping dosages are 5×10^{13} , and $5 \times 10^{15} \text{ cm}^{-2}$, respectively. The crystallization for the F-ions-implanted a-Si film and standard a-Si was realized by excimer laser annealing system. The standard poly-Si TFTs using excimer laser annealing was fabricated to serve as control samples. The re-crystallization was realized by a KrF excimer laser system at room temperature in vacuum ($\sim 0.13 \text{ Pa}$) with laser energy of $300 \text{ mJ}/\text{cm}^2$. After patterning and etching the active region, the 50-nm-thick SiO_2 (tetraethylorthosilicate) and the 200-nm-thick poly-Si gate were both deposited by LPCVD system. The $^{31}\text{P}^+$ ions served as the source/drain ion implantation after patterning and etching the poly-gate. The ion accelerating energy is at 17 keV and the dosage is $5 \times 10^{15} \text{ cm}^{-2}$. The activation was realized by the deposition of the tetraethylorthosilicate passivation layer using LPCVD system at $700 \text{ }^\circ\text{C}$ for 3 h. The contact holes regions were patterned and then etched by buffer oxide etching solution. The aluminum layers was deposited as the metal layers, and then patterned to form metal pads. Finally, the devices are sintered in the thermal furnace at $350 \text{ }^\circ\text{C}$ for 30 min. The device cross-section was shown in the insert of Fig. 1. In this study, all devices investigated have channel length/width of $10 \mu\text{m}/10 \mu\text{m}$.

3. Results and discussion

This study examines the electrical characteristics of F-ions-implanted poly-Si TFTs. Fig. 1 illustrates the transfer characteristics of poly-Si TFTs for F ion implantation dosage of $5 \times 10^{13} \text{ cm}^{-2}$ and standard poly-Si TFTs without F ion implantation. Table 1 summarizes the major TFT device parameters. The threshold voltage (V_{TH}) is defined as the gate voltage yields the

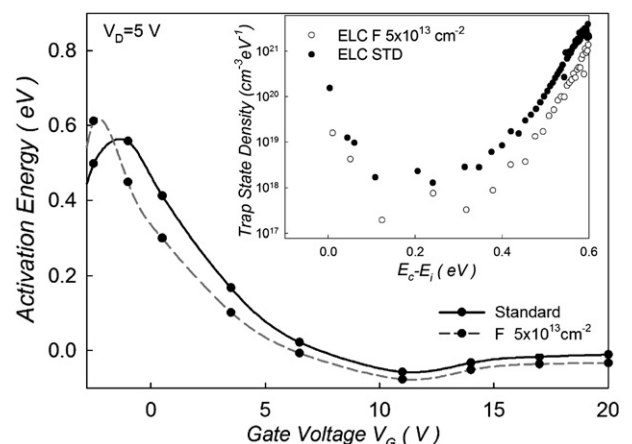


Fig. 2. The activation energy (E_A) of the poly-Si TFTs with and without F ions implantation, as a function of gate voltage. (Drain voltage V_D applied at 5 V). The insert shows the distribution of trap state density in the poly-Si bandgap.

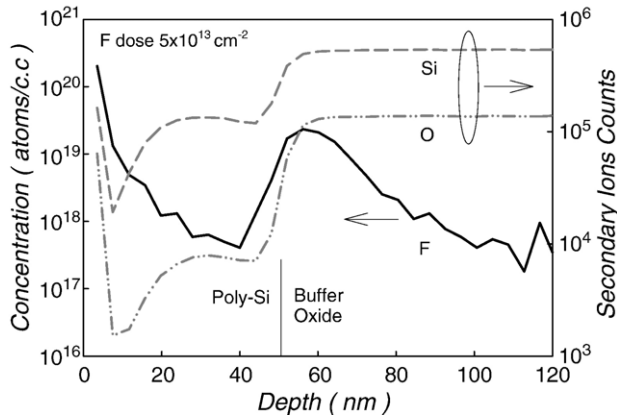


Fig. 3. The secondary ion mass spectrometry (SIMS) analysis of fluorine in the F-implanted poly-Si film after excimer laser crystallization process. The implant dosage of F is $5 \times 10^{13} \text{ cm}^{-2}$.

drain current (I_{DS}) ($I_{DS} = 10 \text{ nA} \times W/L$). The electrical characteristics are improved by F ion implantation at a dose of $5 \times 10^{13} \text{ cm}^{-2}$, particularly for the μ_{FE} and V_{TH} . The μ_{FE} value for F-ions-implanted poly-Si TFTs was twice the magnitude of the standard one ($56.7 \text{ cm}^2/\text{V s}$ to $103.9 \text{ cm}^2/\text{V s}$). The decrease of V_{TH} increased its potential for poly-Si TFTs application, and significantly improved the on-state performance of the F-ions-incorporated poly-Si TFTs. Moreover, the off-state current is also decreased. The improvement of electrical characteristics could be attributed to the reduction of trap states in the poly-Si TFTs. In order to confirm the effect of trap state, activation energy analysis was also executed in this study. From the equation $I_D I_0 e^{\frac{E_A}{kT}}$, using the linear fitting of the $\ln(I_D)$ versus the $1/kT$ plot, in which k is the Boltzmann constant and T is the temperature. Then the activation energy can be extracted [16]. Fig. 2 shows the activation energy (E_A) of drain current as a function of the gate voltage measured at $V_D = 5 \text{ V}$ for the standard and the F-ion-implanted poly-Si TFTs. The E_A was determined by measuring the $I_D - V_G$ characteristic in the temperature range from $20 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$. The activation energy E_A denotes the carrier transportability, which is related to the barrier height in the poly-Si channel [17]. For the F-ion-implanted poly-Si TFTs, the value of E_A

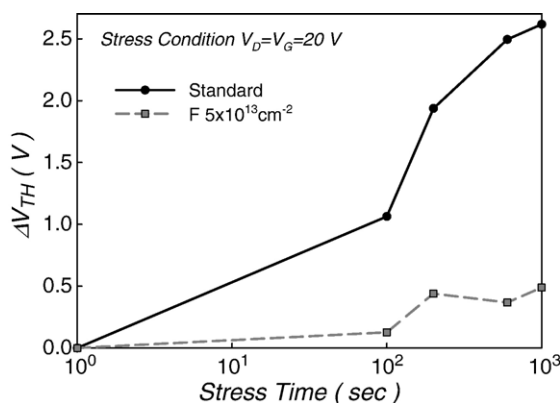


Fig. 4. The threshold voltage variation as a function of stress time, for the standard poly-Si TFTs and F-implanted poly-Si TFTs with ion dosage of $5 \times 10^{13} \text{ cm}^{-2}$.

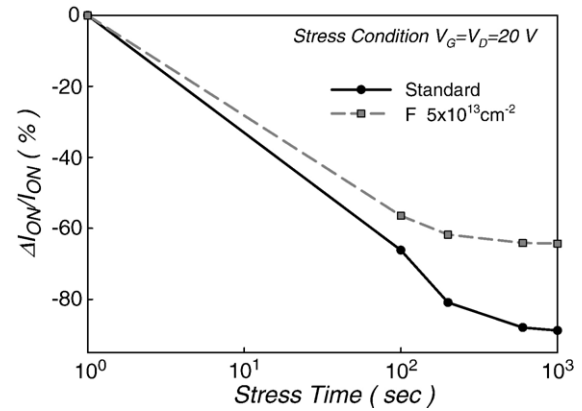


Fig. 5. The on-current variation as a function of stress time for the standard poly-Si TFTs and F-implanted poly-Si TFTs with ion dosage of $5 \times 10^{13} \text{ cm}^{-2}$.

extracted from on-state current is reduced, while E_A extracted from the off-state current is increased, indicating that F-ion implantation effectively reduces the trap state density. Furthermore, the calculated tail states and deep states in the band gap [18] are clearly reduced through the way of F ions passivation, as shown in the insert of Fig. 2. The superior values of s.s., V_{TH} and μ_{FE} for the F-ions-implanted poly-Si TFTs confirm the decrease of trap state density at the interface between poly-Si and oxide. This result is consistent with the above electrical characteristics. The deep trap states can be effectively reduced by using F ions implantation, leading to reduced V_{TH} in n-ch poly-Si TFTs [12]. The fluorine effectively piled up at the interface of poly-Si for active region without the need of pad oxide deposition, as revealed in secondary ion mass spectrometry (SIMS) analysis in Fig. 3. The native oxide of Si film provides F driving force to segregate at the surface during thermal annealing. Therefore, no additional thermal annealing step and manufacture processes were needed to accumulate the F ions. The stronger Si–F bonds are easily formed due to the high electronegativity of F atoms. The accumulated F ions at the surface of poly-Si lower the trap states to achieve good performance of poly-Si TFTs. In addition, the high concentration of F ions between poly-Si and buffer oxide is

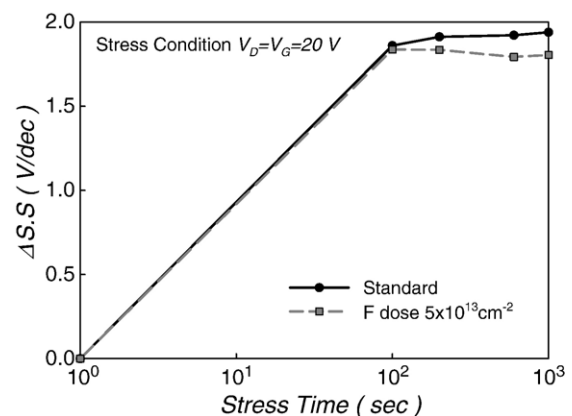


Fig. 6. The subthreshold swing variation as a function of stress time for the standard poly-Si TFTs and F-implanted poly-Si TFTs with ion dosage of $5 \times 10^{13} \text{ cm}^{-2}$.

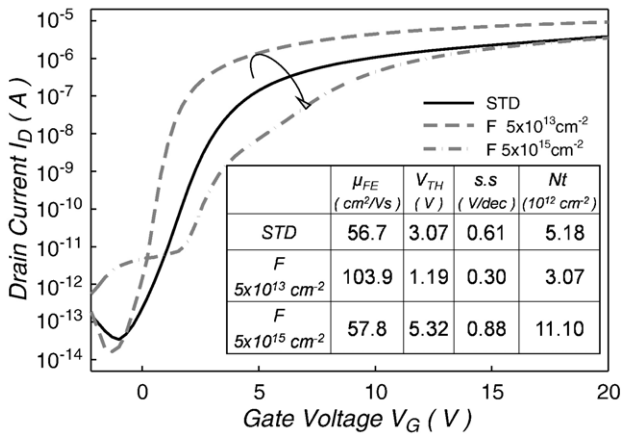


Fig. 7. The transfer characteristics for F-implanted poly-Si TFTs with various ion implantation dosages, compared to the standard poly-Si TFT (Drain voltage V_D applied at 0.1 V).

also found. Hence, the improvement of ELC poly-Si TFTs may be due to the release of mechanical stress at the poly-Si/buffer oxide interface and the passivation effect of fluorine at poly-Si surface.

To examine the device reliability, the poly-Si TFTs were bias-stressed at $V_D=20$ V and $V_G=20$ V for varied time durations of 100 s, 200 s, 600 s and 1000 s. Smaller threshold voltage variation was obtained in F-ion-implanted poly-Si compared to standard poly-Si TFTs, as demonstrated in Fig. 4. Figs. 5 and 6 illustrate the ΔI_{ON} and $\Delta S.S$, respectively, after DC bias stress. Impact ionization multiplication generated from hot carrier effect, near the drain side, degraded the V_{TH} , I_{ON} and S.S, reportedly due to the generation of gate oxide/poly-Si interface states and/or the Si–Si and/or Si–H weak bonds in the

poly-Si channel [19,20]. The F terminated the Si dangling bonds and formed the stronger Si–F bonding endurant to hot carrier degradation, leading to enhanced electrical reliability. The strong Si–F bonds resulting from incorporating F into poly-Si TFTs prevent the bonds from breaking. Hence, F-ions-implanted poly-Si TFTs suffered less degradation of V_{TH} , I_{ON} and S.S than that of conventional poly-Si TFTs.

The electrical characteristics of poly-Si TFTs with heavily high dosage of F ion implantation were also considered in this investigation. The electrical characteristics were degraded as the implantation dosage increased ($5 \times 10^{15} cm^{-2}$). Fig. 7 illustrates the electrical characteristics and the key parameters. The values of μ_{FE} , V_{TH} and S.S for higher F-ions-implanted poly-Si TFTs were degraded as compared to the standard poly-Si TFTs. The trap state density increased as the implantation dosage increased. The segregated fluorine ions in the poly-Si channel will not passivate the trap states, but generate additional defects to degrade the electrical properties. In addition, the fluorine ions are prone to accumulate and form more fluorine clusters during the sequent fabrication process, even worsening the electrical characteristics [21,22]. Moreover, the fluorine elements were found to be highly volatile in high temperature in the process flow, possibly degrading the electrical characteristics [23].

In general, one of possible causes for the improved electrical characteristics of the poly-Si TFTs might be attributed to grain size enhancement. Fig. 8 illustrates the scanning electron microscope (SEM) analysis, demonstrating an obvious difference in grain size between the standard and the F-ion-implanted poly-Si. Hence, in this work it is confirmed that the improvement in the electrical characteristics of F-ions-implanted poly-Si TFTs are originated from the grain size enhancement and F ions passivation. These study results have demonstrated that the

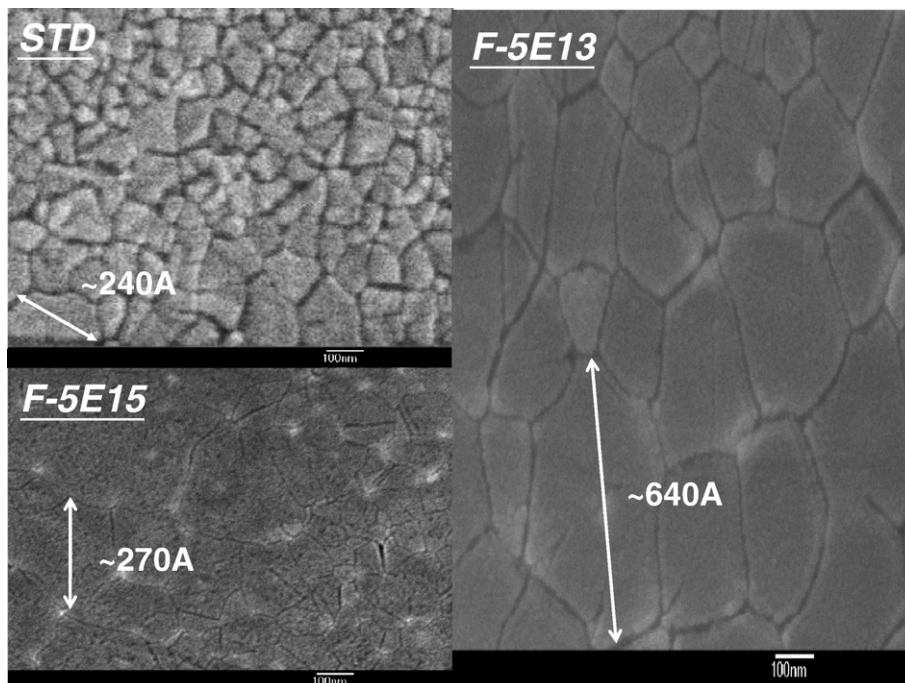


Fig. 8. The scanning electron microscope (SEM) image of the standard and the F-implanted poly-Si films.

degradation of poly-Si TFTs could have originated from the inclusion of F, dependent on the dosage of implanted fluorine.

4. Conclusion

The excimer laser crystallized poly-Si TFTs with F-ions-implantation treatment were fabricated and investigated in this study. Significant improvements in electrical performance and reliability have been obtained with fluorine dose of $5 \times 10^{13} \text{ cm}^{-2}$. The field effect mobility is increased from $56.7 \text{ cm}^2/\text{V s}$ to $103.9 \text{ cm}^2/\text{V s}$ and the threshold voltage is decreased from 3.07 V to 1.09 V. However, the performance will be degraded as the F ions dosage increased in poly-Si film. In our proposed method, the fluorine spontaneously segregates at the poly-Si interface without the procedure of an extra oxide layer deposition, reducing the process step as compared to the conventional fabrication of the F-ion implanted poly-Si TFT. In addition, the proposed technology is compatible with the conventional poly-Si TFTs manufacture process.

Acknowledgment

This work was performed at National Nano Device Laboratory and was supported by the National Science Council of the Republic of China under Contract Nos. NSC 95-2221-E-009-283, NSC 95-2221-E-009-270, NSC 95-2120-M-110-003, and NSC 95-2221-E-009-254-MY2. Also, this work was partially supported by MOEA Technology Development for Academia Project# 94-EC-17-A-07-S1-046.

References

[1] H. Oshima, S. Morozumi, International Electron Device Meeting Technical Digest, 1989, p. 157.

- [2] S.D. Brotherton, *Semicond. Sci. Technol.* 10 (1995) 721.
- [3] K. Nakazawa, *J. Appl. Phys.* 69 (1991) 1703.
- [4] T.J. King, K.C. Saraswat, *IEEE Electron Device Lett.* 13 (1992) 309.
- [5] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, S. Nakano, *Int. Electron Device Meet. Techn. Dig.* 91 (1991) 563.
- [6] T. Sameshima, S. Usui, M. Sekiya, *IEEE Electron Device Lett.* 7 (1986) 276.
- [7] M. Miyasaka, J. Stoemenos, *J. Appl. Phys.* 86 (1999) 5556.
- [8] T. Kuan, A. Chou, J. Kanicki, *Jpn. J. Appl. Phys., Part 1* 38 (1999) 2251.
- [9] D.N. Kouvatso, F.A. Stevie, R.J. Jaccodine, *J. Electrochem. Soc.* 140 (1993) 1160.
- [10] D. Kouvatso, J.G. Huang, R.J. Jaccodine, *J. Electrochem. Soc.* 138 (1991) 1752.
- [11] I.W. Wu, T.Y. Huang, W.B. Jackson, A.G. Lewis, A. Chiang, *IEEE Electron Device Lett.* 12 (1993) 181.
- [12] H.N. Chern, C.L. Lee, T.F. Lei, *IEEE Trans. Electron Devices* 41 (1994) 698.
- [13] J.W. Park, B.T. Ahn, K. Lee, *Jpn. J. Appl. Phys.* 34 (1995) 1436.
- [14] C.H. Tu, T.C. Chang, P.T. Liu, H.W. Zan, Y.H. Tai, C.Y. Yang, Y.C. Wu, H.C. Liu, W.R. Chen, C.Y. Chang, *Electrochem. Solid-State Lett.* 8 (2005) G246.
- [15] C.H. Tu, T.C. Chang, P.T. Liu, C.Y. Yang, H.C. Liu, W.R. Chen, Y.C. Wu, C.Y. Chang, *IEEE Electron Device Lett.* 27 (2006) 262.
- [16] C.A. Dimitriadis, N.A. Economou, P.A. Coxon, *Appl. Phys. Lett.* 59 (1991) 172.
- [17] C.L. Fan, M.C. Chen, *Electrochem. Solid-State Lett.* 5 (2002) G75.
- [18] G. Fortunato, P. Migliorato, *Appl. Phys. Lett.* 49 (1986) 1025.
- [19] S. Banerjee, R. Sundaresan, H. Shichijo, S. Malhi, *IEEE Trans. Electron Devices* 35 (1988) 152.
- [20] M. Hack, A.G. Lewis, I.W. Wu, *IEEE Trans. Electron Devices* 40 (1993) 890.
- [21] T. Sands, J. Ishburn, E. Myers, D.K. Sadana, *Nucl. Instrum. Methods Phys. Res., Sect. B* 7/8 (1985) 337.
- [22] R. Galloni, R. Rizzoli, A. Nylandsted Larsen, S. Yu. Shiryaev, *Nucl. Instrum. Methods Phys. Res., Sect. B* 19/20 (1987) 466.
- [23] J.O. Carlsson, M. Boman, *J. Vac. Sci. Technol.* A3 (1985) 2298.