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Citation: Applied Physics Letters **92**, 122113 (2008); doi: 10.1063/1.2898217
View online: http://dx.doi.org/10.1063/1.2898217
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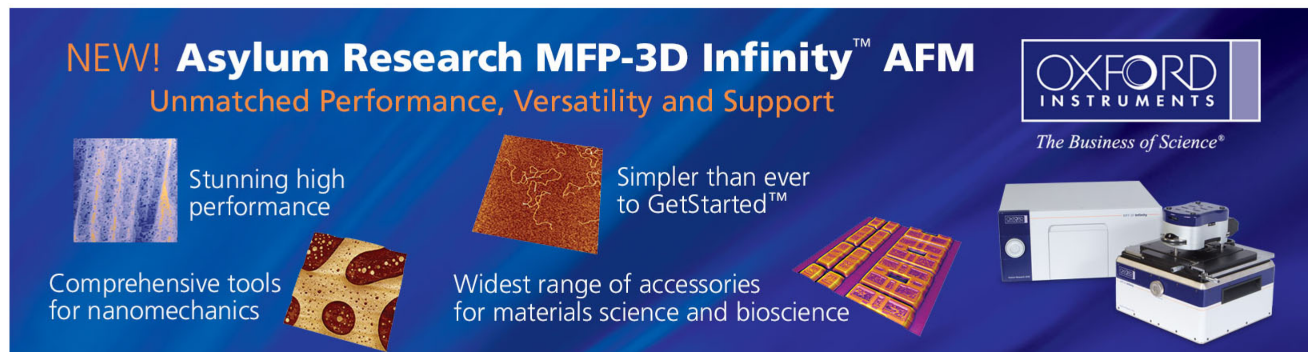

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Anomalous *p*-channel amorphous oxide transistors based on tin oxide and their complementary circuits

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(Received 16 January 2008; accepted 21 February 2008; published online 28 March 2008)

In this article, we report the fabrication of SnO_2 thin film transistors (TFTs) fabricated by reactive evaporation. Different from the previous reports, the fabricated TFTs exhibit *p*-type conductivity in its undoped form. The postdeposition annealing temperature was tuned to achieve *p*-channel SnO_2 TFTs. The on/off ratio and the field-effect mobility were $\sim 10^3$ and 0.011 $cm^2/V\,s$, respectively. To demonstrate inverter circuit, two devices with different threshold voltages were combined and an output gain of 2.8 was achieved. The realization of *p*-channel oxide TFTs would open up new challenges in the area of transparent electronics. © *2008 American Institute of Physics*.
[DOI: 10.1063/1.2898217]

Ever since the demonstration of the first oxide based thin film transistors (TFTs), extensive work has been accomplished in the area of transparent electronics. This is mainly because they are the building blocks of most of the display utilities including the flat panel displays. The transistor arrays were also combined to form inverter and oscillator circuits based on these oxide semiconductors and have already been accomplished on nonsilicon substrates.[1] All the oxide based TFTs reported in the literature to date are *n* channel in nature.[2,3] This is mainly attributed to the oxygen vacancies and the metal ion interstitials which act as donors and, hence, result in the free electrons for the carrier conduction. To date, there are no reports available in the literature on the *p*-type oxide TFTs. Instead, researchers rely on organic materials such as pentacene for the realization of *p*-channel TFTs.[4,5] It has proven to be difficult to achieve *p*-type conductivity in binary oxides such as zinc oxide (ZnO) due to self-compensation effects.[6] Hence, there is a room for the investigation of the *p*-type oxide semiconductors for the future optoelectronic devices. SnO_2 belongs to classic family of oxide semiconductors which combine high electrical conductivity with high optical transparency in the visible region of the electromagnetic spectrum. SnO_2 in its undoped form is *n* type in nature with a wide optical band gap of about 3.6 eV.[7] Efforts have been made in the recent years on the *p*-type SnO_2 by doping with the trivalent aluminum and indium.[8,9] Carrier type conversion from *n* to *p* type was also reported in SnO_2 by the monovalent Li doping.[10] The aforementioned results of the researchers suggest that there is possibility of achieving *p*-type conductivity in SnO_2. Interestingly, the phase diagram of SnO_2 indicates the coexistence of the SnO_2 and SnO phases when the samples were grown near room temperatures. When the oxide exists in such a mixed valence state, there is possibility of *p*-type conduction and such a phase diagram describing the mixed phases has already been reported in literature.[11] Keeping in view of the aforementioned factors, in the present article, the fabrication of *p*-channel TFT was realized using SnO_2 as an active channel layer. The process used for the growth of the TFT was conventional reactive evaporation. It is worth mentioning that the processing temperature and growth technique used in present study could be a very promising low-cost method for the future flexible electronic devices.

Thin films of SnO_2 can be prepared by numerous methods such as molecular beam epitaxy,[12] sol-gel,[13] sputtering,[14]

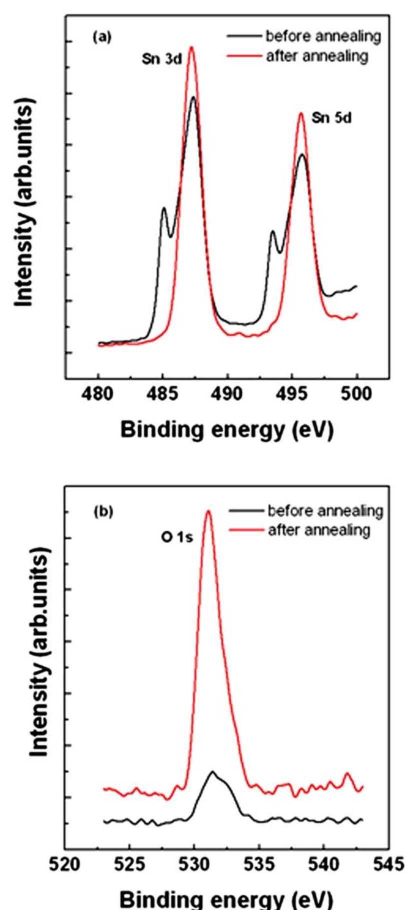

FIG. 1. (Color online) XPS spectra of (a) Sn 3*d* and (b) O 1*s* for the films before and after annealing.

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chemical vapor deposition,[15] etc. We have chosen to focus on reactive evaporation because of its simplicity, easy operation, and relatively minimum critical process parameters. Detailed processing routes of the TFT fabrication is described below. On a routinely cleaned SiO_2 gate dielectric, SnO_2 thin films were deposited by reactive evaporation using Sn as an elemental source and oxygen as a reactive gas. Evaporation in a controlled oxygen environment was possible through a mks mass flow controller. Both evaporation rate and thickness of the film are the critical parameters which decide the TFT characteristics and, hence, were precisely controlled by quartz thickness monitor. While a slow evaporation rate of 0.2 Å/s was maintained during the deposition, the thickness of the films was fixed at 75 Å. Such a slow evaporation rate ensured better reaction of the metal vapors with the oxygen during the evaporation. The as-deposited films were subjected to postdeposition annealing process at a temperature of 100 °C for 1 h. The resultant films were used for the following characterizations. The crystallinity of the films was checked using x-ray diffractometer. The O/Sn ratio and the oxidation state of Sn were determined from x-ray photoelectric spectroscopy (XPS). Once the oxygen rich composition was confirmed, the films were processed for the source-drain metal contacts through thermal evaporation. Silver was used as a metal electrode. Typical channel length and width were 100 and 2000 μm, respectively. The output and transfer characteristics of the TFT were measured using HP 4156 semiconductor parameter analyzer. All the measurements were carried out at room temperature.

The chemical composition of the films before and after heat treatment and the oxidation states of Sn were determined by XPS. Figure 1 displays the Sn 3*d* and O 1*s* XPS spectra of the films before and after annealing. As seen from the Fig. 1, the as-deposited samples exhibited an additional peak corresponding to the Sn^0 state. However, upon annealing, they get transformed to higher oxidation states. The origin of *p*-type conductivity may be ascribed to the nonstoichiometric composition of the sample resulted because of the reactive evaporation and prolonged annealing process. As observed from the XPS analysis it was found that there was drastic change in the composition of the sample upon annealing and the ratio of O/Sn increased from 2.5 to 3.11. This ensured an oxygen-rich environment. The increase in the concentration of oxygen eventually causes a decrease in the concentration of electrons. It has been previously reported in the case of binary systems such as SnO_2 and ZnO that the oxygen enrichment in the sample leads to the *p*-type conduction.[16] Hence, the plausible explanation for origin of holes could be the cation vacancy and interstitial oxygen. Moreover, the mixed valance states of Sn^{2+} and Sn^{4+} could also be one of the contributors for the *p*-type behavior. In the oxygen rich environment, some of the Sn^{2+} will be transformed to Sn^{4+} in order to maintain the charge neutrality. Such a process is equivalent to a hole formation and these holes which locate near the top of the valence band serve as acceptor states, thus, resulting in *p*-type semiconductor. Another plausible reason for the appearance of hole conduction is the grain boundary conduction. It is observed from the atomic force microscopy (AFM) image (Fig. 2) that the grain size of the films was in the range of 40–50 nm. The grains were well separated by a large density of grain boundaries, as shown in Fig. 2. These grain boundaries by virtue of their lower defect formation energy tend to become electron inhibitors and, hence, promote the hole transport. Such a grain boundary dominated transport leading to *p*-type conduction in metal oxide systems such as ZnO are also reported in literature.[17]

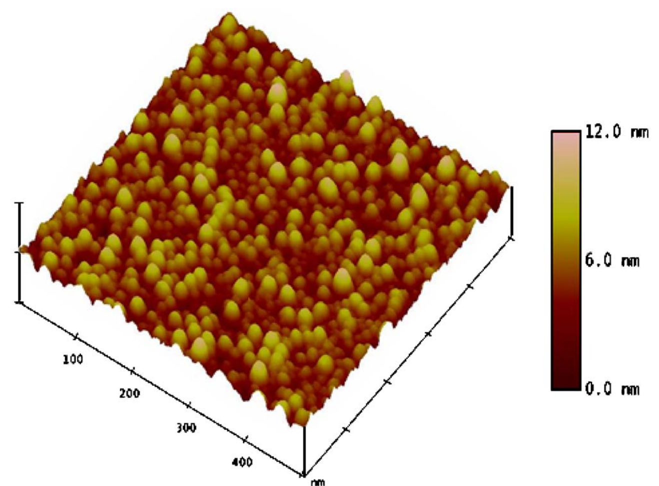

FIG. 2. (Color online) AFM image of SnO_2 thin films annealed at 100 °C.

The as-deposited films were *n* type in nature as observed by the other researchers. Although not shown, the typical *I-V* characteristics exhibited a linear curve depicting Ohmic behavior of the metal-semiconductor contact. The resistivity of the films was calculated from the *I-V* curves and the value was found to be 1.2 Ω cm. Such a resistivity value ensures high electron background concentration and, hence, is not suitable for TFT applications. Hence, postdeposition annealing is found to be crucial in obtaining the *p*-type behavior. The output characteristics of bottom-gate, top-contact SnO_2 TFTs constructed on SiO_2 gate dielectric is displayed in Fig. 3(a). The observed TFT characteristic is typical of a *p*-channel semiconductor, wherein the voltage across the drain to source was modulated by the negative gate bias. The output curves are similar to the conventional transistor models with both linear and saturation regimes. The drain current increased linearly in the lower voltage regions and a clear saturation behavior was observed at high drain voltages because of the pinch off of the accumulation layer. The resistivity of the channel layer was calculated using the output curve in the linear region at a gate voltage of zero and the obtained value was ~160 Ω cm. The output curve at different gate voltages was used to plot the transfer curve [Fig. 3(b)], which is essential for the extraction of the TFT parameters such as field-effect mobility (μ), on/off ratio, threshold voltage (V_{th}), and subthreshold voltage swing. These parameters were extracted using the following relation: $I_{DS} = (\mu C_{OX} W/2L)(V_{GS} - V_{th})^2$, where C_{OX} was the capacitance per unit area of dielectric layer and W and L were the channel width and length, respectively. The slope and intercept of the plot of square root of drain current ($\sqrt{I_D}$) versus gate to source bias (V_{GS}) was used to extract the field effect mobility and threshold voltage and were found to be 30.4 V and 0.011 $cm^2/V\,s$, for the films annealed at 100 °C. The subthreshold voltage swing (S), the voltage required to increase the drain current by a factor of 10, was extracted from the transfer curve using the relation $S = [dV_{GS}/d(\log I_{DS})]$. The obtained S value (~2.0) was used to compute the interface trap density[18] at the semiconductor/dielectric interface and the value obtained was $\sim 8.1 \times 10^{11}/cm^2$. The higher trap

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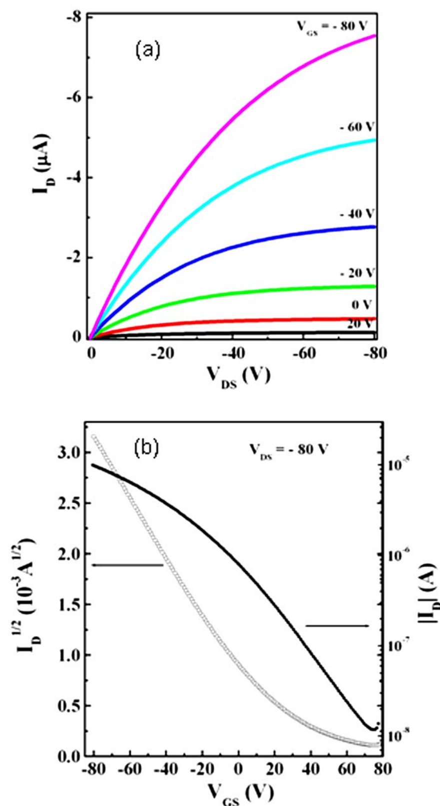

FIG. 3. (Color online) (a) The drain current as a function of drain voltage at various gate voltages for the top-contact SnO_2 TFTs and (b) The transfer curve $[(I_D)^{1/2}-V_{GS}]$ at V_{DS}=−80 V for various gate voltages.

density values could be one of the contributors for the observed low mobility. The lower mobility value was attributed to the scattering of carriers at the grain boundaries and other structural defects arising because of the amorphous nature of the films. The threshold voltage could be tuned by employing higher annealing temperatures. The V_T shifted to 3.72 V for the film annealed at 150 °C for 1 h (data not shown). Such a threshold voltage shift with increased annealed temperature could be attributed to the reduced density of grain boundaries.[19] Two such TFTs of different threshold voltages were used for the construction of the inverter.

A bottom contact inverter structure comprising of two SnO_2 TFTs annealed at different temperatures were constructed and the structure view is shown in inset of Fig. 4. The oxide inverter was constructed by interconnecting two TFTs grown on SiO_2 gate oxide. In order to characterize the fabricated inverter, a supply voltage of −80 V was applied. The measured voltage transfer curves and their corresponding gains are shown in Fig. 4. Ideal voltage transfer curve is expected to have a transition region located near V_{in} $=V_{DD}/2$, where V_{in} is the input voltage and V_{DD} is the supply voltage. It is observed from the transfer curve that the transition region is around half the input voltage. The gain of the inverter was calculated by differentiating the voltage transfer curve and it was found to be around 2.8.

In summary, we have shown that SnO_2 is a promising *p*-channel semiconductor for the optoelectronic devices. Oxygen rich composition, mixed valence states of tin and the grain boundary densities are considered to be the major contributors for the origin of *p*-type behavior. By employing

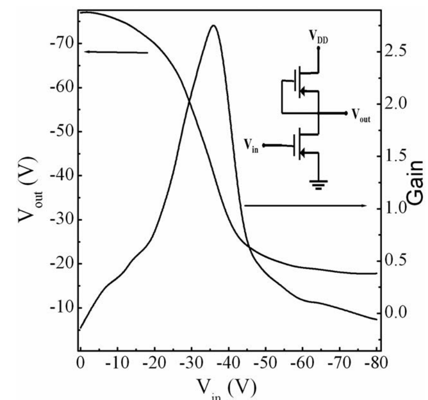

FIG. 4. The measured transfer characteristics of inverter and its corresponding gain at a supply voltage of −80 V. Inset: The schematic of the inverter circuit comprising of two bottom contact SnO_2 TFTs annealed at different temperatures.

devices of two threshold voltages, we have demonstrated the fabrication of complementary inverter. More detailed investigation of the carrier transport in the amorphous oxide is necessary to enhance the device performance. Nevertheless, appearance of *p*-channel SnO_2 TFT adds another dimension to its applications in transparent electronics.

The authors are also grateful to the National Science Council, Taiwan (95-2218-E-001-003 and 96-2628-E-007-030-MY2) and Academia Sinica, Taiwan for financial support.

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