Investigation of Anomalous Inversion *C–V* Characteristics for Long-Channel MOSFETs With Leaky Dielectrics: Mechanisms and Reconstruction

Wei Lee, Pin Su, Ke-Wei Su, Chung-Shi Chiang, and Sally Liu

***Abstract*—This paper investigates anomalous inversion capacitance–voltage (*C–V*) attenuation for MOSFETs with leaky dielectrics. We propose to reconstruct the inversion *C–V* characteristic based on long-channel MOSFETs using the concept of intrinsic input resistance ($R_{\rm ii}$). The concept of $R_{\rm ii}$ has been validated by segmented BSIM4/SPICE simulation. Our reconstructed *C–V* characteristics show poly-depletion effects, which are not visible in the two-frequency three-element method and agree well with the North Carolina State University-CVC simulation results. The intrinsic input resistance dominates the overall gate-current-induced debiasing effect ($\sim$95% for $L = 20\,\mu$m) and can be extracted directly from the *I–V* characteristics. Due to its simplicity, our proposed $R_{\rm ii}$ approach may provide an option for regular process monitoring purposes.**

***Index Terms*—Capacitance–voltage (*C–V*), intrinsic input resistance, metal–oxide–emiconductor (MOS) capacitance, MOSFET, ultrathin gate oxide.**

I. Introduction

THE gate capacitance–voltage (*C–V*) characteristic is fundamental to CMOS technology development because it plays an important role in oxide thickness extraction [21], carrier mobility calculation, interface trap characterization, and so on. As the gate dielectric thickness is reduced (below 20 Å), the inversion *C–V* characteristic is distorted due to direct tunneling current [1]–[19]. Since the gate-tunneling current in metal–oxide semiconductor (MOS) test structures may result in a significant distributed channel resistance effect [5]–[9], several studies proposed conducting *C–V* measurements using short-channel devices [1]–[9], [14]–[19]. Fig. 1(a) shows the observed inversion *C–V* characteristic with adequate calibrations for short-channel devices. Although the inversion *C–V* characteristic is acceptable for gate bias ($V_{\rm GS}$) smaller than 1 V, there still is significant *C–V* distortion for $V_{\rm GS} > 1$ V. One general way to solve this problem is to increase the *C–V* measurement frequency [14]–[18]. Based on the frequency-dependent characteristics, parasitic component effects can be excluded and true *C–V* characteristics can then be calculated by a certain model of choice. For example, Pantisano *et al.* [15] proposed a *C–V* measurement from 1 kHz to 100 MHz and an extraction methodology using the three-element model [3], [4], [22], [23]. However, *C–V* measurements in the high-frequency range require high frequency probes [ground–signal–ground (GSG)] and RF test structures. Moreover, the calibration procedures in high-frequency measurements and model-data fitting make the *C–V* reconstruction rather time consuming for regular product monitoring. Besides, using these short-channel devices in *C–V* measurements has several drawbacks such as small intrinsic capacitance, large parasitic components, and uncertainty in the physical gate length. In other words, the variation of measured capacitance increases as channel length decreases [Fig. 1(b)]. Therefore, the reconstruction of *C–V* characteristics from long-channel devices is still a crucial issue.

Several studies have constructed the *C–V* characteristics for long-channel devices using distributed circuit approaches [5]–[9]. For example, Barlage *et al.* [7] proposed using a transmission line concept to extract the inversion MOS capacitance. In [5], we employed segmented SPICE simulation with each subtransistor modeled by the BSIM4 MOSFET model to simulate the anomalous *C–V* curves due to gate tunneling. Although these methods may provide well-restored characteristics, the implementation is too complicated to be routinely used in a technology development. To develop a simple method for the inversion *C–V* reconstruction, the challenge lies in capturing the distributed nature of the gate capacitance and the channel resistance in a compact way. This is analogous to the gate input impedance modeling in the compact model development for RF CMOS, where an intrinsic input resistance has been introduced [10] as a major part of the gate input resistance. In this paper, we investigate the inversion *C–V* reconstruction and assess the feasibility of the concept of intrinsic input resistance for long-channel MOSFETs.

This paper is organized as follows. In Section II, we describe our *C–V* measurements and BSIM4-based macro model using in this paper. In Section III, we identify dominant mechanisms responsible for the inversion *C–V* attenuation in long-channel devices. In Section IV, we investigate the validity of the concept of intrinsic input resistance. In Section V, we assess the feasibility of the intrinsic input resistance approach for the inversion *C–V* reconstruction. The conclusion will be drawn in Section VI.

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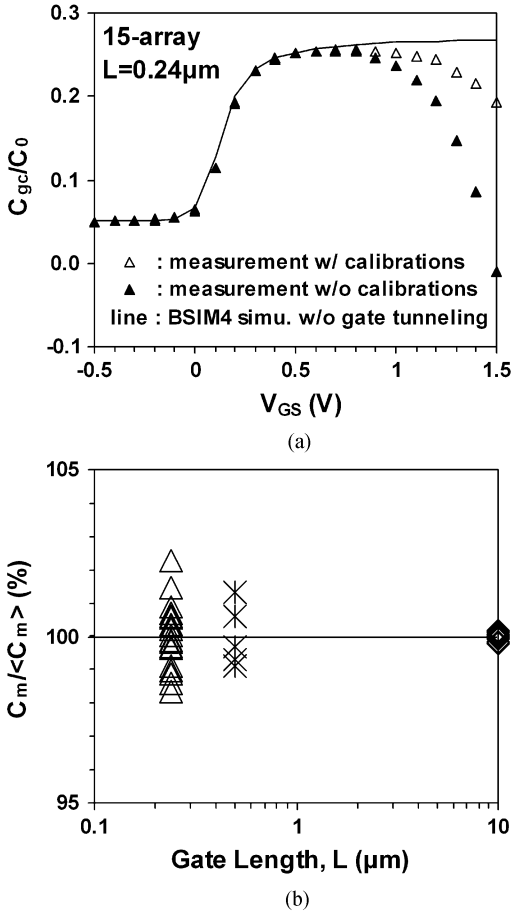

Fig. 1. (a) Inversion MOS capacitance ($C_{\rm gc}$) for short-channel ($L = 0.24\mu$m) device. C_0: true capacitance for $L = 10\mu$m. (b) Variation of $C_{\rm m}$ increases as L decreases. $C_{\rm m}$: measured capacitance. $<C_{\rm m}>$: $C_{\rm m}$ mean.

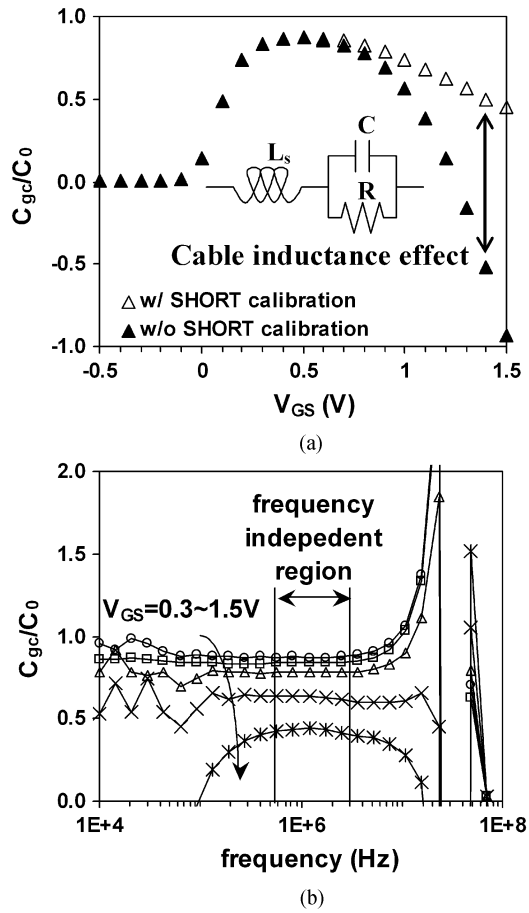

Fig. 2. (a) Impact of cable inductance, $L_{\rm s}$, on $C_{\rm gc}$. (b) Frequency dependence of measured $C_{\rm gc}$.

II. Device, Measurement, and Simulation

Standard MOSFETs with doped poly-Si gate electrode were fabricated and tested. The equivalent oxide thickness (EOT) is about 11 Å. The transistor gate length (L) ranges from 0.24 to 10 μm with 10-μm width (W). For the short-channel device with $L = 0.24\,\mu$m, we employed a test structure with 15-array devices in parallel. Our *C–V* measurement was carried out using the impedance analyzer Agilent 4294A and the Cascade Microtech probe system (S300 series) with DCP 100 probes. Under the RC parallel mode, the Hi port of Agilent 4294A was connected to source/drain, while the Lo port was connected to the gate electrode (SD-G case). The measurement principle of Agilent 4294A is the four-terminal pair (4TP) configuration with the auto-balancing-bridge (ABB) method [13]. In the 4TP configuration, the outer shield of leads of Agilent 4294A needs to be connected together to provide a current return path to cancel the magnetic field generated by the inner current loop [13]. Besides, the whole system of the *C–V* measurement needs to be isolated from actual ground to exclude complicated coupling effects from the ground path and maintain stability of the *C–V* measurement.

Although the cable inductance, $L_{\rm s}$, can be removed to a certain extent in the 4TP configuration [13], residual inductance may result in negative capacitance. Fig. 2(a) shows the measured inversion MOS capacitance, $C_{\rm gc}$, with and without an adequate SHORT calibration. Without performing the SHORT calibration, $C_{\rm gc}$ dramatically drops as $V_{\rm GS}$ increases. By an adequate SHORT calibration, the residual $L_{\rm s}$ ($\sim 1\ \mu$H in series, Fig. 2(a) inset) can be compensated. In addition, $L_{\rm s}$ and stray capacitances may induce a resonance when the measurement frequency increases [13]. As shown in Fig. 2(b), a resonance at $\sim$30 MHz can be seen. The resonance leads to not only accuracy degradation but also very unstable measurement. To avoid the impact of the resonance, we performed *C–V* measurements in the frequency-independent region [Fig. 2(b)]. It is worth noting that the instrumentation error [19] and the impact of extrinsic capacitances and resistances [1]–[3] are frequency dependent. Therefore, measuring $C_{\rm gc}$ in the frequency-independent region may avoid these two mechanisms. In other words, the attenuation in $C_{\rm gc}$ measured in the frequency-independent region with adequate calibrations [Δ in Fig. 2(a)] can be attributed to mechanisms of the intrinsic device part. After excluding the influences from the extrinsic components in the measurement setup, the $C_{\rm gc}$ data was then used in the following BSIM4-based extraction methodology.

Fig. 3(a) shows the BSIM4-based macro model we used in the simulation of $C_{\rm gc}$. Segmented SPICE simulation that divides the transistor along the length direction with ten subtransistors in series was utilized and the BSIM4 device model pa-

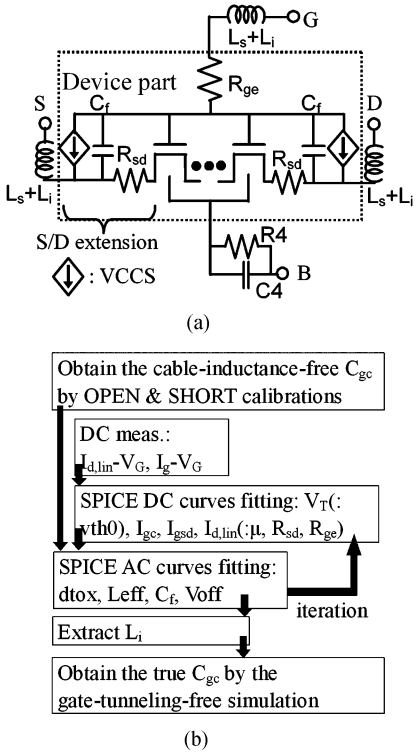

Fig. 3. (a) BSIM4-based macro model. C_f: fringing capacitance. $R_4 = 1 \times 10^9\,\Omega$, $C_4 = 1 \times 10^{-9}$ F. (b) Our BSIM4 extraction methodology of inversion MOS capacitance.

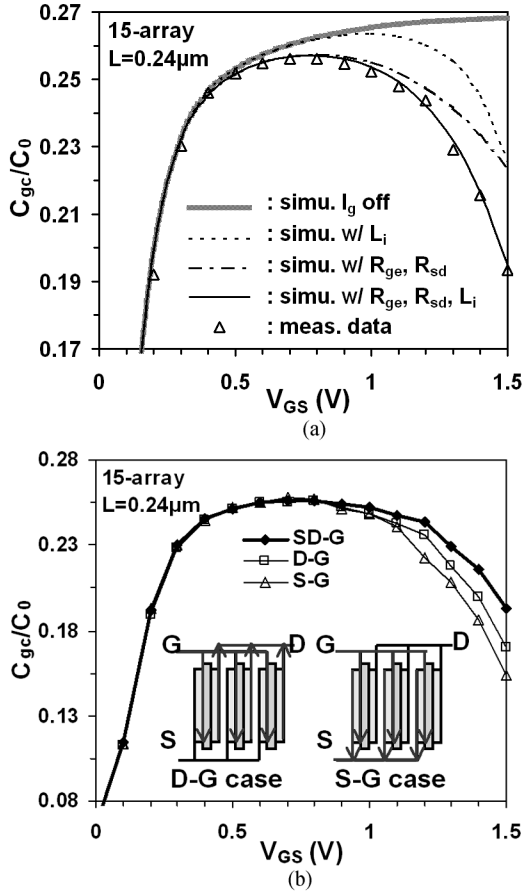

Fig. 4. (a) Merely considering $R_{\rm ge}$ and $R_{\rm sd}$ without taking $L_{\rm i}$ into account cannot model $C_{\rm gc}$ characteristics in high gate bias regime. (b) In same MOS array of short-channel devices, impact of on-chip inductance (L_i) depends on measurement configuration. (For SD-G case, Hi port is connected to source/drain, while Lo port to the gate electrode.)

rameters were calibrated through our extraction methodology [Fig. 3(b)]. Our $C_{\rm gc}$ extraction methodology considers both dc and ac characteristics of devices. Basic device dc parameters such as threshold voltage (V_T), gate tunneling current (I_g), mobility (μ), and source/drain resistance $(R_{\rm sd})$ need to be first determined and used in the ac analysis of SPICE. The oxide thickness, effective channel length, gate electrode resistance $(R_{\rm ge})$, and the parasitic inductance within the test structure itself (L_i) can then be extracted based on a comparison between the $C_{\rm gc}$ data and the simulation results. The true inversion MOS capacitance can be obtained by the gate-tunneling-free simulation.

III. Mechanisms

In this section, we discuss various mechanisms associated with the intrinsic device responsible for the anomalous *C–V* characteristics.

A. Short Channel Device

Fig. 4(a) shows significant capacitance attenuation in the $C_{\rm gc}$ measurement for the device with $L = 0.24\,\mu$m. The parasitic effects caused by $R_{\rm ge}$, $R_{\rm sd}$, and L_i are responsible for the attenuation. Note that the impact of source/drain resistance $R_{\rm sd}$ and gate electrode resistance $R_{\rm ge}$ increases as L decreases. In addition, the short-channel test structure is usually designed as a multi-array type to increase the impedance of the capacitor. As a result, the residual on-chip inductance $L_{\rm i}$ may become significant in the multi-array test structure when large current exists. By comparing the $C_{\rm gc}$ measurement data with the L_i-free simulation [Fig. 4(a)], it can be seen that the L_i effect is significant in the high gate bias (i.e., high gate tunneling) regime. Moreover, the $L_{\rm i}$-induced $C_{\rm gc}$ attenuation depends on the measurement configuration. As shown in Fig. 4(b), various measurement configuration may result in various $C_{\rm gc}$ attenuation due to a different current direction. In other words, different *C–V* characteristics may be observed for the multi-array test structure with the same size but different layout. Therefore, the $L_{\rm i}$ effect increases the uncertainty in the *C–V* measurement for short-channel devices.

B. Long-Channel Device

Regarding the capacitance attenuation for the long-channel device, the impact of the gate-tunneling-induced distributed effect is crucial. Because of the IR drop caused by gate-tunneling current, the channel potential is a distribution instead of a constant. Moreover, this potential distribution depends on $V_{\rm GS}$, L, and measurement configuration. Fig. 5(a) shows the channel potential distribution at $V_{\rm GS} = 1.5$ V for the device with $L = 10\,\mu$m. For the SD-G case (Hi port to Source/Drain, Lo port to Gate), the maximum potential $\sim$0.17 V occurs at the center of the channel, because of the symmetric gate-tunneling current from gate to source/drain. For the D-G case (the Hi port to the drain electrode only), however, the maximum potential

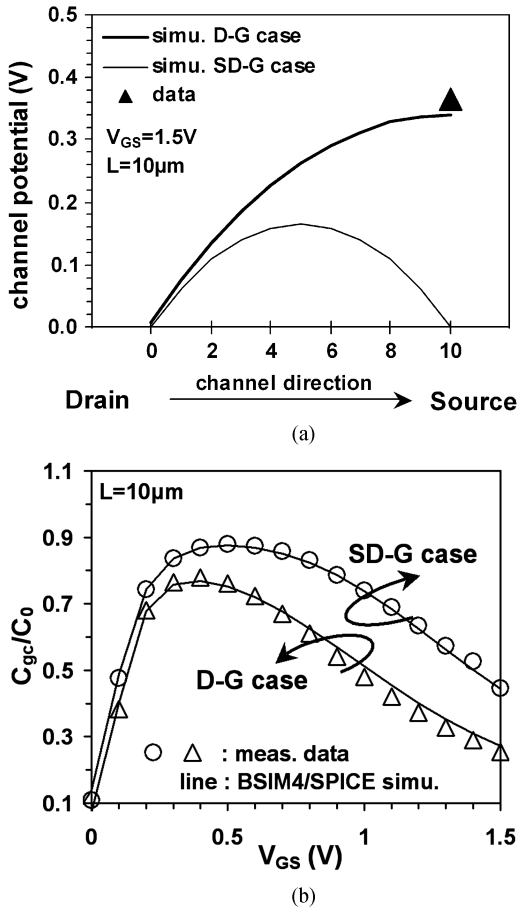

Fig. 5. (a) DC and (b) AC verification of the segmented SPICE simulation for distributed effect.

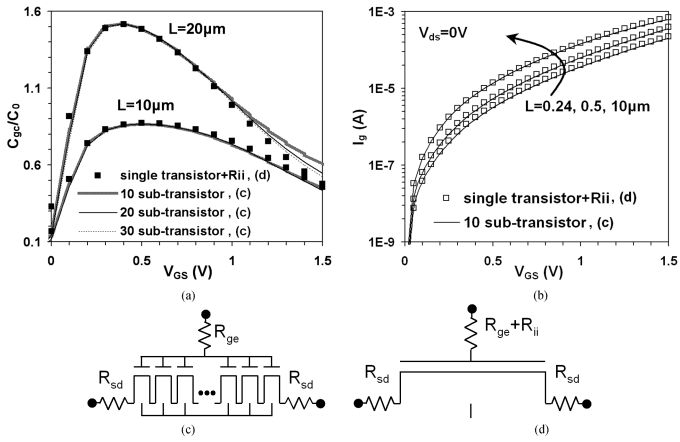

Fig. 6. (a) Gate-tunneling-induced *C–V* attenuation due to debiasing effect can be simulated by BSIM4/SPICE simulation. (b) Gate currents simulated by segmented simulation and $R_{\rm ii}$ lumped simulation are nearly identical. (c) Segmented SPICE simulation with each subtransistor modeled by BSIM4 MOSFET model. (d) Single-transistor SPICE simulation with $R_{\rm ii}$ added to gate terminal in addition to $R_{\rm ge}$.

$\sim$0.34 V occurs at the floating side (source side). It is worth noting that both the maximum IR drop and the capacitance attenuation [Fig. 5(b)] are enhanced in the D-G case. The excellent model-data fit in Fig. 5(b) shows the accuracy of our BSIM4-based segmented SPICE simulation.

IV. Intrinsic Input Resistance Model

Fig. 6(a) shows BSIM4/SPICE-simulated *C–V* characteristics for devices with leaky dielectrics. The BSIM4 device model parameters are the same as those used in Figs. 4 and 5. As shown in Fig. 6(a), a substantial attenuation in the inversion capacitance for long-channel MOSFETs can be seen. The attenuation results mainly from the gate-tunneling-induced debiasing effect. Also shown in Fig. 6(a) is that a single-transistor simulation with an intrinsic input resistance, $R_{\rm ii}$, added to the gate terminal in addition to gate electrode resistance [Fig. 6(d)] yields nearly identical results as those of segmented simulation with sufficient (e.g., 30) subtransistors [Fig. 6(c)]. Besides, the gate currents $(\mathrm{I_g})$ simulated by segmented simulation and the single-transistor simulation with $R_{\rm ii}$ are nearly identical for the devices with $L = 0.24$ to 10 μm [Fig. 6(b)]. It indicates that the tunneling resistance $(dI_g/dV_{\rm gs})^{-1}$ of a single-transistor simulation with $R_{\rm ii}$ is nearly identical to that of segmented simulation.

$R_{\rm ii}$ represents a channel-reflected gate resistance and can be thought of as an equivalent resistance accounting for the first-order non-quasi-static effect in the channel [10], [12]. $R_{\rm ii}$ is proportional to the total channel resistance with a proportional constant α, which accounts for the distributed effect of the complex RC network constructed by the gate capacitance and the channel resistance. Since this RC network has a short termination at both source and drain nodes in the *C–V* measurement, α can be approximated as 1/12 because the location at which the gate current equals zero occurs at L/2 [12]. The channel resistance and $R_{\rm ii}$ have been modeled through channel integration in BSIM4 [10], [12] and can be extracted from the measured *I–V* [Fig. 7(a)]. Fig. 7(b) shows that $R_{\rm ii}$ depends on $V_{\rm GS}$ and L. As L increases, $R_{\rm ii}$ increases.

Fig. 6 indicates that the $R_{\rm ii}$ approach is accurate and efficient in simulating the distributed effect in long-channel MOSFETs. For the device with $L = 10\,\mu$m, it can be seen from Fig. 6(a) that ten subtransistors are enough to capture the distributed effect. For the device with $L = 20\,\mu$m, however, ten subtransistors are not sufficient to gain satisfactory accuracy. There is significant discrepancy between the two $C_{\rm gc}$ curves with 10 and 20 subtransistors. It is worth noting that as the number of subtransistors increases, the $C_{\rm gc}$ curves of the segmented simulation are close to that of the $R_{\rm ii}$ lumped simulation. In other words, the uncertainty in selecting the number of subtransistors to simulate the distributed effect can be avoided by the $R_{\rm ii}$ lumped simulation. Therefore, using the $R_{\rm ii}$ approach in the inversion *C–V* reconstruction for long-channel MOSFETs is more accurate and efficient than the segmented-simulation approach.

V. Reconstruction

In this section, we demonstrate that the concept of $R_{\rm ii}$ can be used to develop a simple method for the inversion *C–V* reconstruction for long-channel devices. As the conventional three-element model [Fig. 8(a)] is used to represent the small-signal equivalent model of a leaky MOS capacitor, the total series resistance, $R_{\rm s}$, can be calculated by $R_{\rm ii}+R_{\rm ge}+R_{\rm sd}/2$. The factor

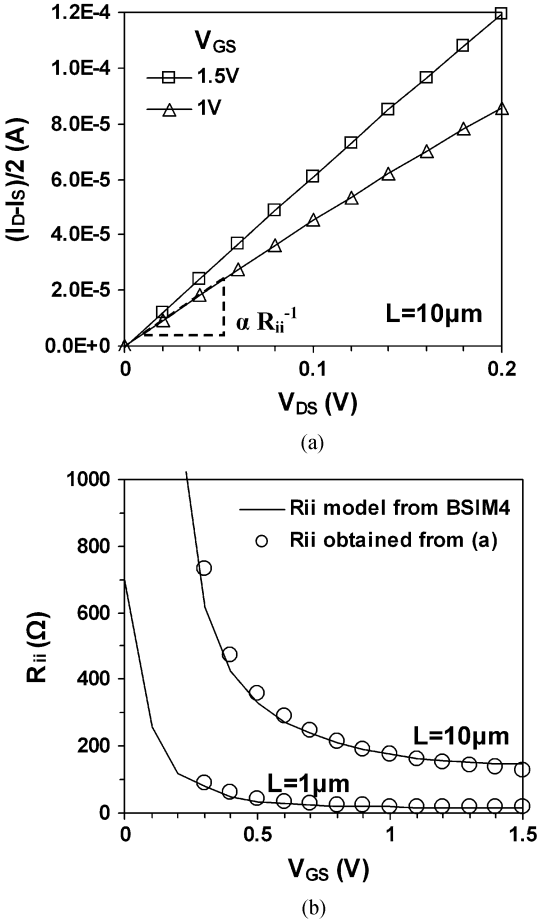

Fig. 7. (a) $R_{\rm ii}$ for $L = 10\,\mu$m device can be extracted from dc output characteristics. (b) $R_{\rm ii}$ as a function of $V_{\rm GS}$ and L.

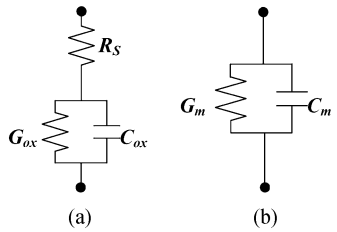

Fig. 8. Small-signal equivalent models for MOS capacitor. (a) Three-element model. (b) Two-element parallel model.

of 1/2 accounts for the $R_{\rm sd}$-induced debiasing effect caused by one half of $\rm I_g$. The inversion *C–V* may then be reconstructed by [20], [23]

$$C_{\rm OX} = \frac{C_m}{(1 - G_m R_s)^2 + \omega^2 C_m^2 R_s^2} \tag{1}$$

where $\rm C_m$ and $\rm G_m$ represent the measured capacitance and conductance, respectively, using the parallel circuit model of the LCR meter [Fig. 8(b)]. The value of $R_{\rm ii}$ can be extracted from the channel resistance [Fig. 7(a)]. The values of $R_{\rm ge}$ and $R_{\rm sd}$ can also be measured by standard procedures.

Fig. 9(a) and (b) shows the measured inversion capacitance and our reconstructed *C–V* characteristics for NMOS and

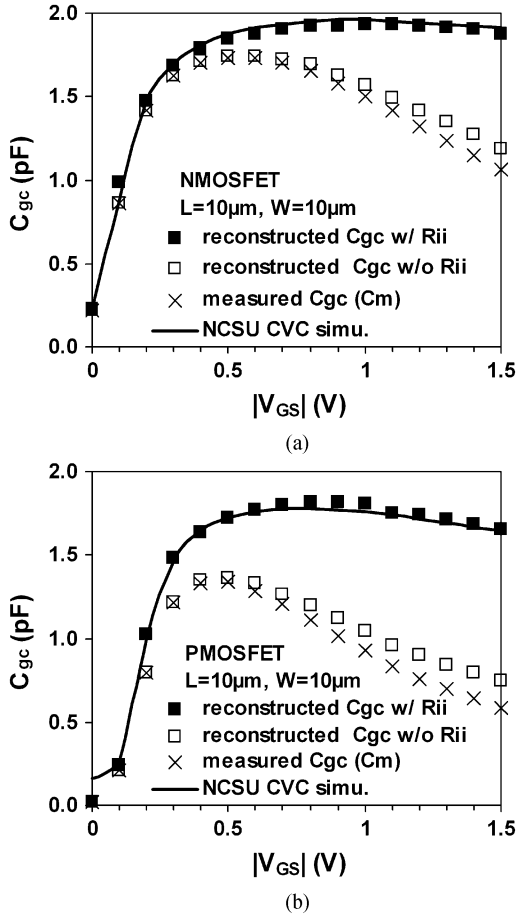

Fig. 9. Reconstructed *C–V* characteristics for (a) NMOS and (b) PMOS with and without considering $R_{\rm ii}$. Results agree well with simulation results of NCSU CVC. ($\rm T_{OX} = 1.15$ nm. NMOS : $\rm N_{Bulk} = 3E17$ $\rm cm^{-3}$, $\rm N_{Gate} = 1.8E20$ $\rm cm^{-3}$, $R_{\rm ge} + R_{\rm sd}/2 = 40\,\Omega$. PMOS : $\rm N_{Bulk} = 2.5E17$ $\rm cm^{-3}$, $\rm N_{Gate} = 8.5E19$ $\rm cm^{-3}$, $R_{\rm ge} + R_{\rm sd}/2 = 180\,\Omega$.)

PMOS with $L = 10\,\mu$m and $\rm W = 10\,\mu$m, respectively. The impact of $R_{\rm ii}$ on the reconstructed results can be seen. Moreover, the correction for PMOS is larger because the lower PMOS channel mobility may result in a higher channel resistance and $R_{\rm ii}$. Besides, the reconstructed *C–V* characteristics show a slight decrease in the high gate bias regime. This can be attributed to poly-depletion effects. Also shown in Fig. 9 are the theoretical characteristics provided by the North Carolina State University CVC (*C–V* analysis software) [14]. Note that merely using the two-frequency three-element method [3], [4], [22], [23] has been known [7], [14] to be unable to show the poly-depletion effect because of the limited number of elements. Using the $R_{\rm ii}$ approach to fully account for the distributed effect together with the three-element model, however, our reconstructed *C–V* curves show poly-depletion effects and agree with the NCSU-CVC simulation results well.

To assess the importance of intrinsic input resistance to the overall gate-current-induced debiasing effect, Fig. 10 shows $R_{\rm ii}/R_s$ as a function of L. It can be seen that the impact of $R_{\rm ii}$ increases with L. For the device with $L = 10\,\mu$m, $R_{\rm ii}/R_{\rm s}$ is $\sim$80%. For $L = 20\,\mu$m, the $R_{\rm ii}/R_s$ ratio can reach as high as 95%. In other words, the inversion *C–V* can be reconstructed

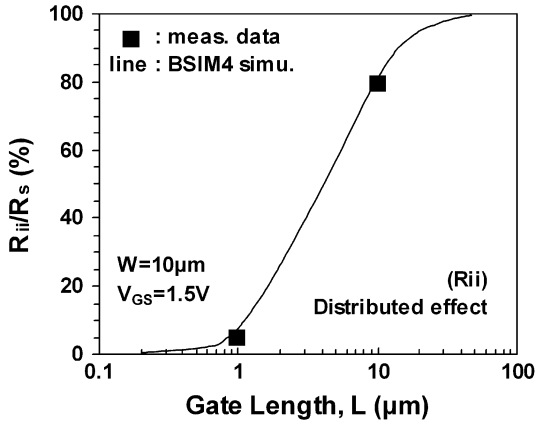

Fig. 10. Contribution of intrinsic input resistance in overall gate-current-induced debiasing effect. $R_{\rm s} = R_{\rm ii} + R_{\rm ge} + R_{\rm sd}/2$.

by (1) with $R_s \approx R_{\rm ii}$, which can be obtained from the channel resistance extraction shown in Fig. 7(a).

VI. Conclusion

We have investigated the inversion *C–V* reconstruction and assessed the feasibility of the concept of intrinsic input resistance for long-channel MOSFETs. The concept of $R_{\rm ii}$ has been validated by segmented BSIM4/SPICE simulation. Using the $R_{\rm ii}$ approach in the inversion *C–V* reconstruction is more accurate and efficient than the segmented simulation approach. Our reconstructed *C–V* characteristics show poly-depletion effects and agree well with the NCSU-CVC simulation results. The intrinsic input resistance dominates the overall gate-current-induced debiasing effect ($\sim$95% for $L = 20\,\mu$m) and can be extracted directly from the *I–V* characteristics. Due to its simplicity, our proposed $R_{\rm ii}$ approach may provide an option for regular process monitoring purposes.

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