Bidirectional Current-Mode Capacitor Multipliers for On-Chip Compensation

Ke-Horng Chen, Chia-Jung Chang, and Te-Hsien Liu

***Abstract*—Single-ended and two-ended bidirectional capacitor multipliers for providing on-chip compensation, soft-start, and fast transient mechanisms are proposed in this paper. The bidirectional current mode capacitor multiplier technique can effectively move the crossover frequency toward to the origin in the start-up period for a smoothly rising of the output voltage. Besides, the small time constant is set by the fast transient control circuit in order to get a higher crossover frequency. Thus, the output voltage can be regulated to its stable value as fast as it can when large load current changes. A test chip fabricated by the Taiwan Semiconductor Manufacturing Corporation (TSMC) 0.35-μm process verifies the correctness of the bidirectional current mode capacitor multiplier technique. Experimental results demonstrate the transient speed by our proposed technique is faster than that by conventional control by about 2 times, and there is only about 76% dropout voltage of the conventional design with off-chip compensation. The proposed circuits consume more quiescent current about 10 μA in single-ended capacitor multiplier and 20 μA in two-ended capacitor multiplier. With the proposed bidirectional current mode capacitor multiplier technique, the performance of dc-dc converters is improved significantly and the external pins and footprint area are minimized.**

***Index Terms*—Capacitor multiplier, compensator, current mode, dc-dc converter, on-chip compensation.**

I. Introduction

PALM-sized devices like cellular phones, personal digital assistants, digital cameras, music players, and other multimedia entertainments demand highly integrated circuits. Higher level of integration yields better performance resulted from a reduction of parasitic components of bonding wires, connections, or package. Unfortunately, off-chip inductors and capacitors take up significant area on PCBs, add production cost, and obstruct system-on-chip (SoC) applications. For the sake of reducing harmful effects of bonding wire parasitic elements and power loss on them, making all the circuits to be on-chip becomes a matter of concern. High integration is necessary for achieving high performance and small footprint area in portable equipments today.

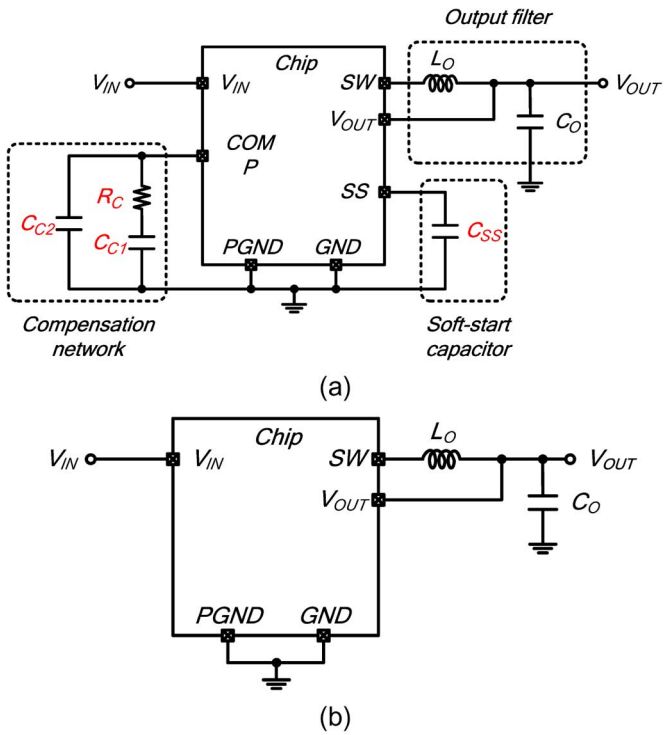

Fig. 1. (a) Typical application circuit for dc/dc buck converter with current mode control. (b) Proposed dc/dc buck converter with minimized external pins and components

As we know, it is imperative to integrate large off-chip compensation and soft-start capacitors in Fig. 1 into the chip for minimizing external pins and footprint area. In Fig. 1, the conventional compensation network contains a resistor R_C and capacitors C_{C1} and C_{C2}; the soft-start mechanism contains a capacitor C_{SS}. Thus, after the integration of these passive components, the chip can have minimized external pins and need only the output filter, which contains an inductor L_o and a capacitor C_o. If the integration of the output filter into the chip is needed, the technique of system-in-package (SIP) can be used to implement the large off-chip output filter [1], [2].

Thus, for low cost and high integration, a bidirectional current mode capacitor multiplier technique to implement a buck converter with minimized external pins and high performance is proposed. In other words, the functions of compensation, soft-start, and fast transient response are achieved by the proposed bidirectional current mode capacitor multiplier technique at the same time. It means that only a low-cost and bidirectional current mode capacitor multiplier technique is used to eliminate the

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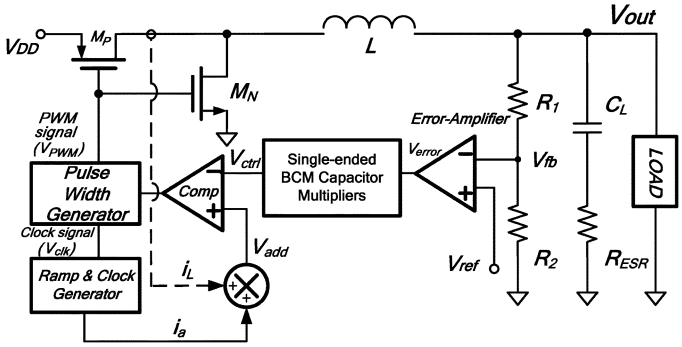

Fig. 2. Current-mode dc-dc converter with the proposed bidirectional current mode capacitor multiplier technique.

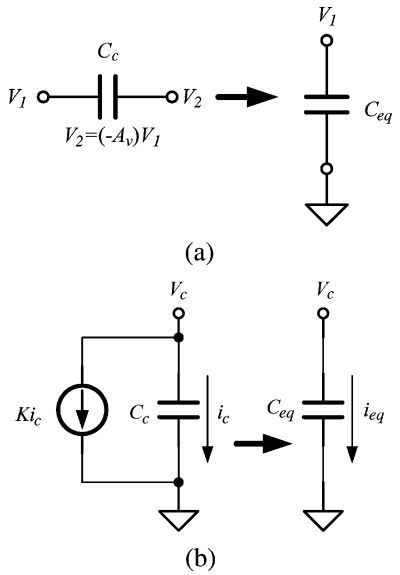

Fig. 3. Capacitor multiplier techniques. (a) Voltage mode. (b) Current mode.

demand of external pins ($COMP$ and SS). Besides, owing to the bidirectional current mode capacitor multiplier technique, the output overshoot/undershoot voltage in case of load variations is smaller than that of conventional design.

The difficulty of high integration in the design of dc-dc converters is due to the large off-chip capacitors of proportional integration (PI) compensation and soft-start function. PI compensation technique [3]–[6] achieves a popular pole-zero cancellation for compensating current mode buck dc-dc converters. The compensator must generate a pair of pole-zero to counteract the dominant pole and form a new suitable dominant pole for the designed bandwidth. However, large-valued capacitors needed for compensation often occupy substantial space. Thus, in order to not occupy large silicon area, the high integration is achieved by modifying the time constant. Under the deliberate control procedure of error amplifier, the response of error amplifier is increased in case of large load variations and decreased in case of start-up process. At normal operation, the control circuit works as a current mode Miller multiplier for achieving large on-chip capacitance in order to implementing lag compensation (PI compensation). It means that minimizing the size of capacitors can alleviate the tradeoff between cost and performance thereby maximizing profit.

The bidirectional current mode capacitor multiplier technique contains the functions of on-chip compensation, soft-start, and fast transient response is proposed in this paper. The circuit analysis and implementation is proposed in Section II. Importantly, in order to improve the performance of the dc-dc converters, the time constant is adaptively modified for dynamically changing the crossover frequency. Smooth soft-start period and fast transient recovery are achieved by the single-ended bidirectional capacitor multiplier technique. In Section III, the concept of the single-ended capacitor multiplier technique is extended to two-ended technique for the implementation of type II compensator. The test chip is fabricated by TSMC 0.35 μm process and experimental results are shown in Section IV. Finally, a conclusion is made in Section V.

II. Single-Ended Bidirectional Current Mode Capacitor Mulitplier Technique

The single-ended bidirectional current mode capacitor multiplier technique is shown in Fig. 2. Observe that the bidirectional current mode capacitor multiplier circuit implements the functions of compensation, soft-start procedure, and fast transient response. In the presence of the bidirectional current mode capacitor multiplier circuit, the external components that contain output filter (L, C) and feedback resistors (R_1, R_2) are minimized owing to the on-chip compensation and soft-start capacitors. Thus, the low-cost buck converter with minimized external pins is achieved by the proposed technique. The output of our proposed buck converter output contains only an output filter (L, C). It means that the converter needs a small footprint area and, correspondingly, a low cost.

A. Voltage-Mode and Current-Mode Miller Capacitances

Generally speaking, there are two techniques [7] to get an equivalent capacitor, one technique is so-called voltage-mode and the other is current-mode. Based on the Miller theorem, the equivalent capacitor is equal to the original value multiplied by a factor $(1 + A_v)$ if the voltage of one terminal of the capacitor is $(-A_v)$ times that of the other terminal as shown in Fig. 3(a). The equivalent value of capacitor is as

$$C_{eq} = (1 + A_v)C_c. \tag{1}$$

The other popular current-mode technique of capacitor multipliers is shown in Fig. 3(b). The concept is to sense the current through a small capacitor, then amplify and bypass this amplified current across the two terminals of the small capacitor. Therefore, the equivalent capacitor is derived by the following equations:

$$\begin{aligned} i_c &= C_c\frac{dv_c}{dt} \Rightarrow (K+1)i_c = (K+1)C_c\frac{dv_c}{dt} \\ C_{eq} &= (K+1)C_c \end{aligned} \tag{2}$$

Several capacitor multiplier circuits have been proposed [7]–[11]. There is a voltage-mode Miller capacitor multiplier applied in phase-locked loops needs a negative gain amplifier

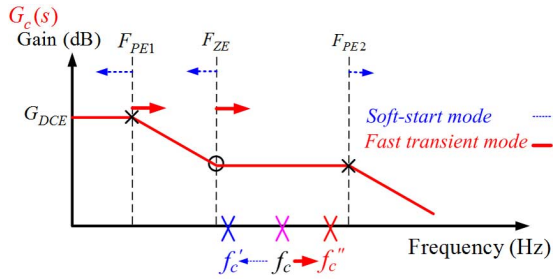

Fig. 4. Frequency response of the bidirectional current mode capacitor multiplier circuit.

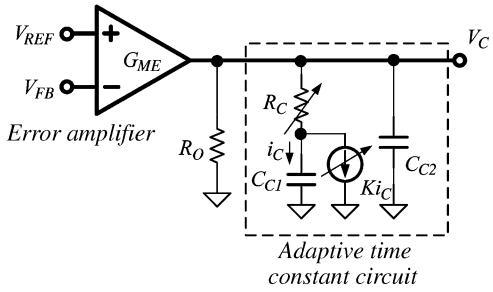

Fig. 5. Symbolic description of the proposed time constant technique.

[11]. Besides, the amplifier must have no input dc current because such a dc current results in large leakage and voltage spur. Therefore, a noninverting amplifier followed by a negative unity gain buffer is necessary, although there is still a leakage current flowing through feedback resistors. However, one important design restriction is that large multiplication factor may induce severe gain compression. Because when the input of operational amplifier experiences large voltage swing, its output voltage is limited by power rails. Consider a current-mode capacitor multiplier [7] used in a single-stage amplifier that is used an output stage of operational amplifier. Traditional Miller compensation could be accomplished by this multiplied capacitor. However, current mirrors can only amplify one direction of the current flowing through the small capacitor, so extra dc bias currents are necessary for this technique. The summary is that the capacitor multiplier is needed to have the characteristics, which are no dc current consumption, large signal swings, and little silicon area.

B. Analysis of the Single-Ended Capacitor Multiplier for On-Chip Compensation, Soft-Start, and Fast Transient Operations

Fig. 4 shows the frequency response of the bidirectional current mode capacitor multiplier technique. The plot is similar to the lag compensation with a higher frequency pole for alleviating the high noise effect. Thus, it contains two poles (F_{PE1}, F_{PE2}) and one zero (F_{ZE}) [3], [4]. It is interesting and useful to observe that the effective crossover frequency different from that of normal operation at start-up and fast transient operation. As we know, the crossover frequency (f_c) should be extended to a higher frequency (f_c'') at fast transient operation. However, it should to be moved to a lower frequency (f_c') at start-up operation. In other words, the bidirectional current mode capacitor multiplier circuit modifies the positions of two poles and one zero to a suitable frequency positions. In the meanwhile, the operation of the proposed bidirectional current mode capacitor multiplier technique makes sure the stability of the system.

Fig. 5 illustrates the symbolic description of the proposed bidirectional current mode capacitor multiplier circuit. The dynamic current source is to generate an equivalent current whose value is K times the current (i_C) flowing through the compensation capacitor C_{C1}. It means that the equivalent series capacitance is increased to be large enough to generate a low-frequency pole-zero pair F_{PE1} and F_{ZE}. For the soft-start operation, the equivalent capacitance is larger than that at the normal operation. Besides, the value of R_C is smaller than that of the normal operation for a large separation between the pole F_{PE1} and the zero F_{ZE}. In fact the effective crossover frequency is close to the origin for achieving a lower bandwidth. Large time constant makes sure the smooth increase in the output voltage of the error amplifier. Therefore, the soft-start function can prevent the output voltage from overshooting by such a large time constant.

Contrarily, small time constant increases the response of the error amplifier in case of load variations. Thus, the bidirectional current mode capacitor multiplier technique decreases the equivalent capacitance in order to move the pole-zero pair to higher frequency as shown in Fig. 4. In the meanwhile, the effective crossover frequency (f_c) is moved to a higher frequency (f_c'') to get a large bandwidth. However, the utmost importance that we should watch out for is the stability of the system. Thus, the large bandwidth with small phase margin lasts for a short period and the crossover frequency comes back the original value at the normal operation. Fast transient response is achieved by a small time constant and the stability is assured by the control of large time constant period [12], [13].

The single-ended bidirectional current mode capacitor multiplier technique makes sure the smooth operation of soft-start and the fast transient response in case of load variations. The following subsections describe the implementation of the proposed single-ended bidirectional current mode capacitor multiplier technique.

C. Implementation of the Single-Ended Capacitor Multiplier

The implementation of the adaptive capacitance is shown in Fig. 6(a). Two transistors, M_{S1} and M_{S2}, biased in triode region works as two resistances R_{S1} and R_{S2}. The ratio that is the aspect ratio of transistor M_{S2} is divided by that of transistor M_{S1} is K. It means that the current flowing through the transistor M_{S2} is K times that of transistor M_{S1}. Thus, an equivalent capacitance is got by the value of the capacitor C_{C1} multiplied by K. The equivalent small-signal model is shown in Fig. 6(b). Z_{of} and g_m are the open-loop output resistance and transconductance of the voltage follower [14], [15], respectively. The voltage follower implementation is shown in Fig. 6(c) [15]. According to the analysis of literature [16], the transfer function

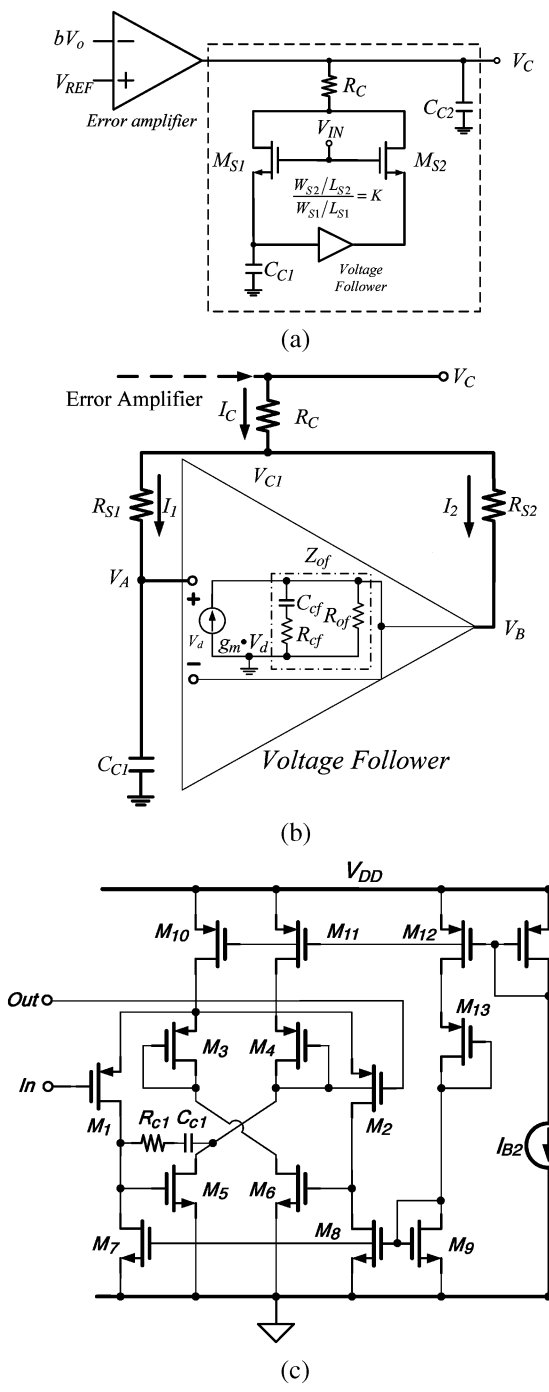

Fig. 6. Implementation of an adaptive capacitance circuit for achieving a variable capacitance at different operation modes. (a) The design of circuit. (b) The small-signal model of the circuit. (c) The schematic of the voltage follower used in the capacitor multiplier.

V_B/V_A and the current ratio I_1/I_2 are described as (3) and (4), respectively,

$$\frac{V_B}{V_A} = \frac{(1+g_m R_{s2}) + sC_{c1}R_{s1}}{(1+g_m R_{s2}) + \frac{R_{s2}}{Z_{of}}} \tag{3}$$

$$\frac{I_1}{I_2} = \frac{R_{s2} + \frac{Z_{of}}{1+g_m Z_{of}}}{R_{s1} + \frac{1}{sC_{c1}}\left(1 - \frac{g_m Z_{of}}{1+g_m Z_{of}}\right)} \tag{4}$$

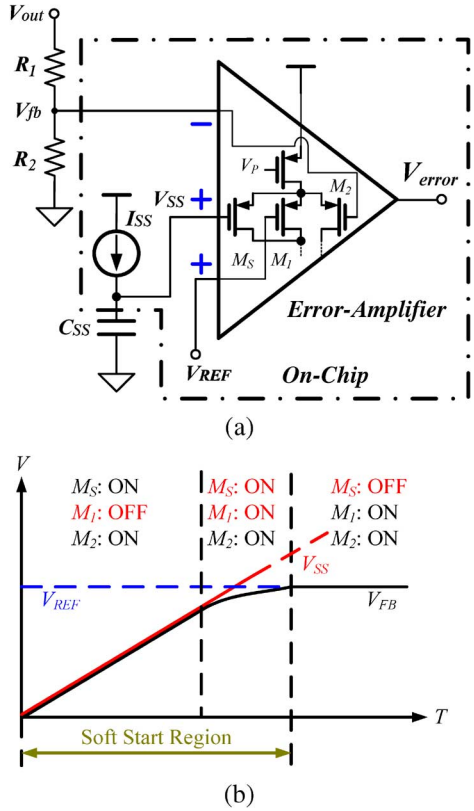

Fig. 7. Conventional soft-start circuit of dc/dc converters. (a) The circuit implementation. (b) The operation regions of the three input transistors in the modified amplifier for soft-start.

If $Z_{of} \gg R_{S2}$ and $g_m R_{S2} \gg 1$, (3) and (4) are approximated as (5) and (6), respectively,

$$\frac{V_B}{V_A} \approx 1 + \frac{sC_{c1}R_{s1}}{g_m R_{s2}} \tag{5}$$

$$\frac{I_1}{I_2} \approx \frac{R_{s2}}{R_{s1}}. \tag{6}$$

Thus, the equivalent input impendence for capacitor multiplier can also be approximated as

$$Z_{IN} \approx \frac{V_{c1}}{I_c} = \frac{(1+sC_{c1}R_{s1})}{sC_{c1}\left(1+\frac{R_{s1}}{R_{s2}}\right)}. \tag{7}$$

The equivalent input resistance Z_{IN} generates a low-frequency pole-zero pair. However, if the resistance R_{S2} is too small, the approximation is not valid. Hence, an offset value exists in the capacitor multiplier and may cause the capacitor multiplier mechanism inaccurate.

D. Implementation of the Soft Start in the Bidirectional Current Mode Capacitor Multiplier Technique

The conventional soft-start circuit is shown in Fig. 7(a) [4]. The large soft-start capacitor C_{SS} and the small bias current I_{SS} make sure the voltage V_{SS} smoothly ramps up the output voltage. Thus, the transistor M_S is added to the input differential stage of error amplifier to substitute for the role of reference voltage $V_{\rm REF}$. When V_{SS} is smaller than $V_{\rm REF}$, the transistor

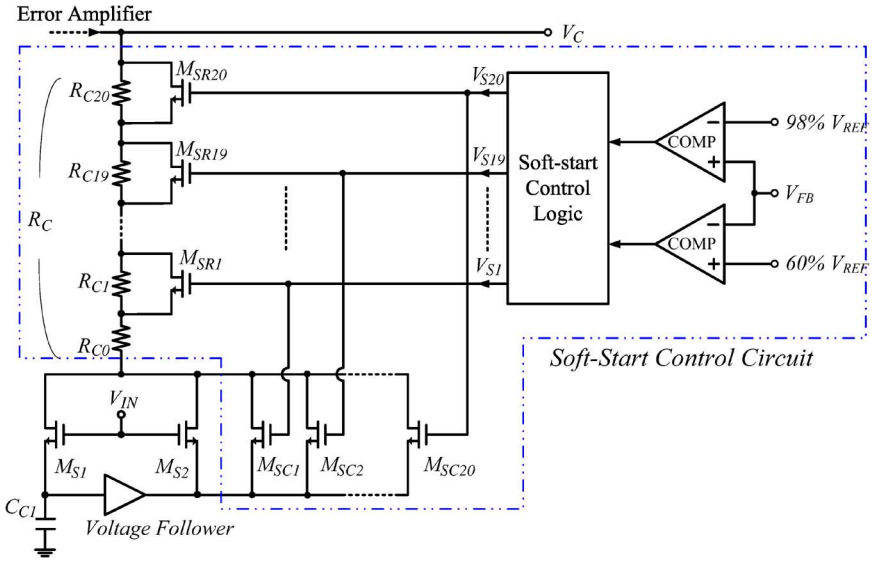

Fig. 8. Proposed bidirectional current mode capacitor multiplier technique with the function of soft-start.

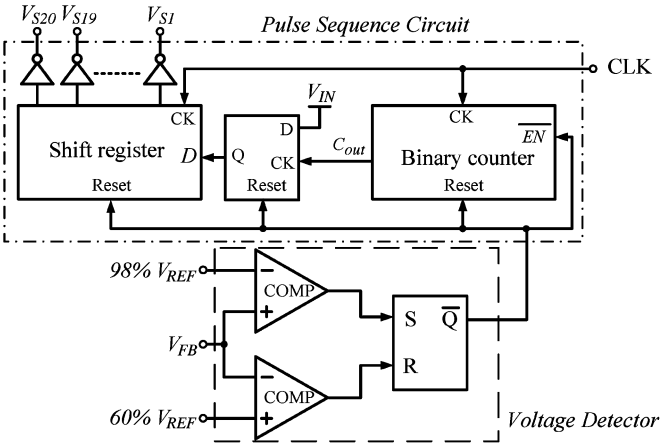

Fig. 9. Soft-start control logic in the proposed bidirectional current mode capacitor multiplier circuit.

M_1 is off and the transistors M_S and M_2 comprise the differential input pair; hence, the error amplifier regulates V_{FB} to V_{SS}. When V_{SS} approaches $V_{\rm REF}$, transistor M_1 starts to conduct, and transistor M_S turns off gradually. Once V_{SS} is high enough, the transistor M_S is completely turned off, and transistors M_1 and M_2 then regulate V_{FB} to $V_{\rm REF}$. The operation regions of the three input transistors are shown in Fig. 7(b). However, the transition from soft start period to normal operation is not smooth in conventional design because there are two control signals $V_{\rm REF}$ and V_{SS} are compared to the feedback voltage V_{FB}. Thus, an overshoot is observed in conventional design. It is of utmost importance to get a large time constant for implementing the function of soft start.

In order to implement the function of soft-start, the bidirection current mode capacitor multiplier circuit is modified as Fig. 8. The resistor R_C in Fig. 5 is divided into small resistors $R_{C0} \sim R_{C20}$, and its value is determined by the aspect ratio of transistors $M_{SR1} \sim M_{SR20}$. Hence, the more the switches are turned on, the smaller the value of R_C. Besides, the equivalent capacitance is also increased by turning on the switches $M_{SC1} \sim M_{SC20}$ to decrease the value of time constant. Because the separation of the pole-zero pair is needed, all the switches are turned on at the beginning of start-up period. It promises the effective crossover frequency is located at a lower frequency than that at normal operation. When the feedback voltage V_{FB} is larger than 98% $V_{\rm REF}$, the soft-start control logic generates a sequence of pulses to turn off the switches $M_{SR1} \sim M_{SR20}$ and $M_{SC1} \sim M_{SC20}$ in sequence to return the value of time constant back to that at normal operation. Owing to the small time constant, the smooth increase of the output voltage is achieved by the modified time constant circuit in Fig. 8.

Fig. 9 illustrates the soft-start control logic circuit. Two comparators are used to determine the start and stop points of soft-start mechanism. One comparator compares the feedback voltage V_{FB} with 60% $V_{\rm REF}$ to decide the start point of soft start function. The time constant is increased to a large value to get a smaller crossover frequency f_c' in Fig. 4. Furthermore, it maintains this large time constant until the feedback voltage V_{FB} is larger than 98% $V_{\rm REF}$. Then, the second comparator sends logic high to SR latch to start the pulse sequence circuit. The pulse sequence circuit provides a smooth transition from soft start operation to the normal pulse width modulation operation. In other words, the crossover frequency f_c' at soft start operation is moved back to f_c at the normal operation. The pulse sequence circuit is enabled by the output SR-latch and generates a carry out $C_{\rm out}$ to trigger the shift register. Thus, the shift register sets the values of $V_{S1} \sim V_{S20}$ from high to low in sequence for decreasing time constant. In the meanwhile, the crossover frequency f_c' is smoothly moved back to the value of f_c at the normal operation. Owing to the smooth transition of crossover frequency, the overshoot of the output voltage can be alleviated. In other words, the bidirectional current mode capacitor multiplier technique with soft-start mechanism can effectively alleviate the inrush current of the inductor.

E. Fast Transient Mechanism in the Bidirectional Current Mode Capacitor Multiplier Technique

Contrarily, the time constant is needed to be decreased when load changes. A small time constant moves the crossover fre-

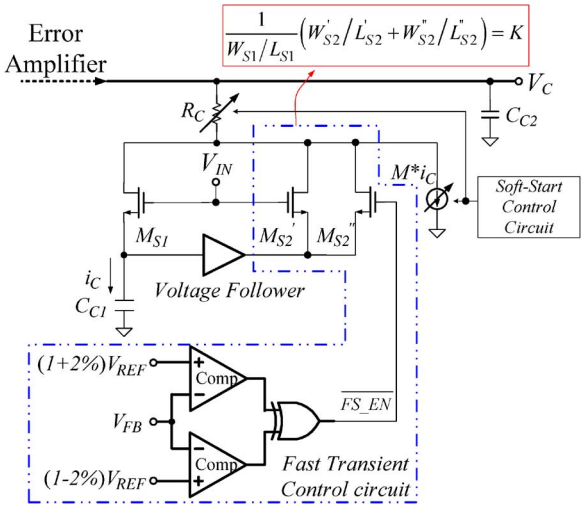

Fig. 10. Proposed bidirectional current mode capacitor multiplier technique with fast transient mechanism.

quency f_c to a higher frequency f_c'' for achieving a fast transient response [12], [13]. However, what we need to take care is the stability of the system because of the higher crossover frequency has less phase margin. Thus, two comparators are used to detect the start time of the fast transient function and prevent the output voltage from ringing. The fast transient mechanism is stopped when the difference between the feedback voltage V_{FB} and the reference voltage $V_{\rm REF}$ is within $\pm 2\%$ $V_{\rm REF}$. Once the output voltage drops lower than $V_{\rm REF}$ about 2% or rises higher than $V_{\rm REF}$ above 2%, the fast transient circuit starts to decrease the time constant. The equivalent resistance R_{S2} in Fig. 6(b) generated by the transistor M_{S2} is divided into two small transistors M'_{S2} and M''_{S2} in Fig. 10. Besides, the sum of the two aspect ratios of transistors M'_{S2} and M''_{S2} is equal to that of the original transistor M_{S2} in Fig. 6(a). The gate of transistor M''_{S2} is set to low when the fast transient function starts in order to get a small equivalent capacitance. Then, the system has a wider bandwidth (f_c'') in Fig. 4 to get a fast response. The phase margin of this fast transient operation is kept larger 45° in order to make sure the stable regulation of output voltage.

III. Two-Ended Bidirectional Current-Mode Capacitor Multiplier Technique

Owing to the previous analysis of the single-ended bidirectional current mode capacitor multiplier technique, the concept can be extended to the two-ended capacitor multiplier technique.

A. Two-Ended Capacitor Multiplier in Type II Compensator

Fundamental type II compensator is composed of an error amplifier, two resistors R_1, R_2 and two capacitors C_1, C_2 as

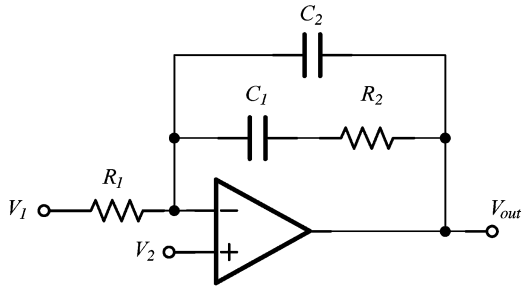

Fig. 11. Typical type II compensator.

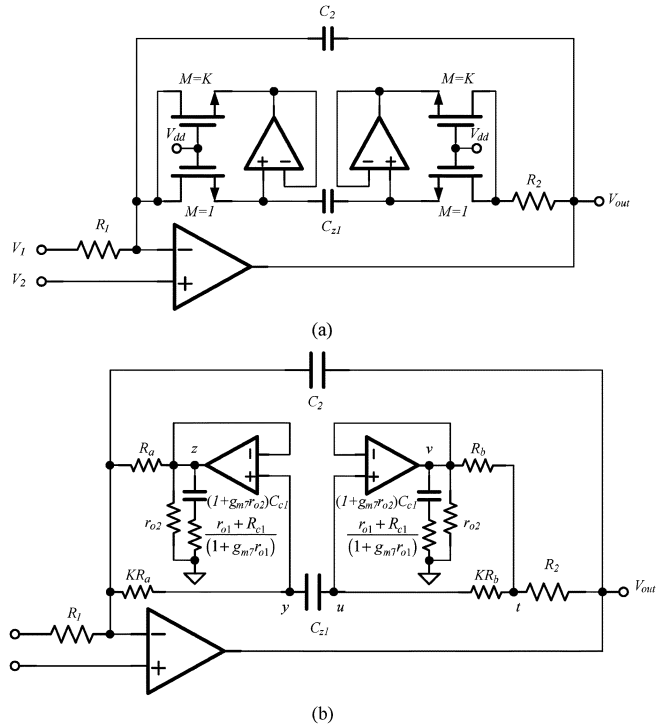

Fig. 12. (a) Proposed architecture of two-ended capacitor multiplier within type II compensator. (b) Equivalent circuit of proposed two-ended bidirectional capacitor multiplier within type II compensator.

shown in Fig. 11. The transfer function of the fundamental type II compensator is given by (8). Replacing this fundamental type II compensator by the proposed two-ended capacitor multiplier is shown in Fig. 12(a). The similar operation of both terminals is that the small signal current flowing through both sides of small capacitor C_{Z1} is multiplied by the same amplification factor K. Therefore, capacitor C_1 could be replaced by the small capacitor C_{Z1} and proposed two-ended bidirectional capacitor multiplier. The equivalent circuit of proposed two-ended capacitor multiplier within type II compensator is shown in Fig. 12(b). The voltage follower is also modeled to have a single-pole (p_1) response. The transfer function of the implementation circuit in Fig. 12(b) is derived as (9) at the bottom of the page.

$$T(s)\approx -\left(\frac{R_2+r_{o2}+g_{m0}Rr_{o2}}{C_{z1}KRR_1r_{o2}g_{m0}s}\right)\times\left[\frac{1+\frac{C_{z1}g_{m0}KRR_2r_{o2}}{(R_2+r_{o2}+g_{m0}Rr_{o2})}s+\frac{C_{c1}C_{z1}g_{m0}kRR_2r_{o1}r_{o2}}{(R_2+r_{o2}+g_{m0}Rr_{o2})}s^2+\frac{2C_{c1}C_{z1}g_{m7}KRR_2r_{o1}r_{o2}}{p_1(R_2+r_{o2}+g_{m0}Rr_{o2})}s^3}{1+C_2R_2s+C_2C_{c1}R_2r_{o1}s^2+\frac{2C_2C_{c1}g_{m7}R_2r_{o1}}{g_{m0}p_1}s^3}\right] \quad (9)$$

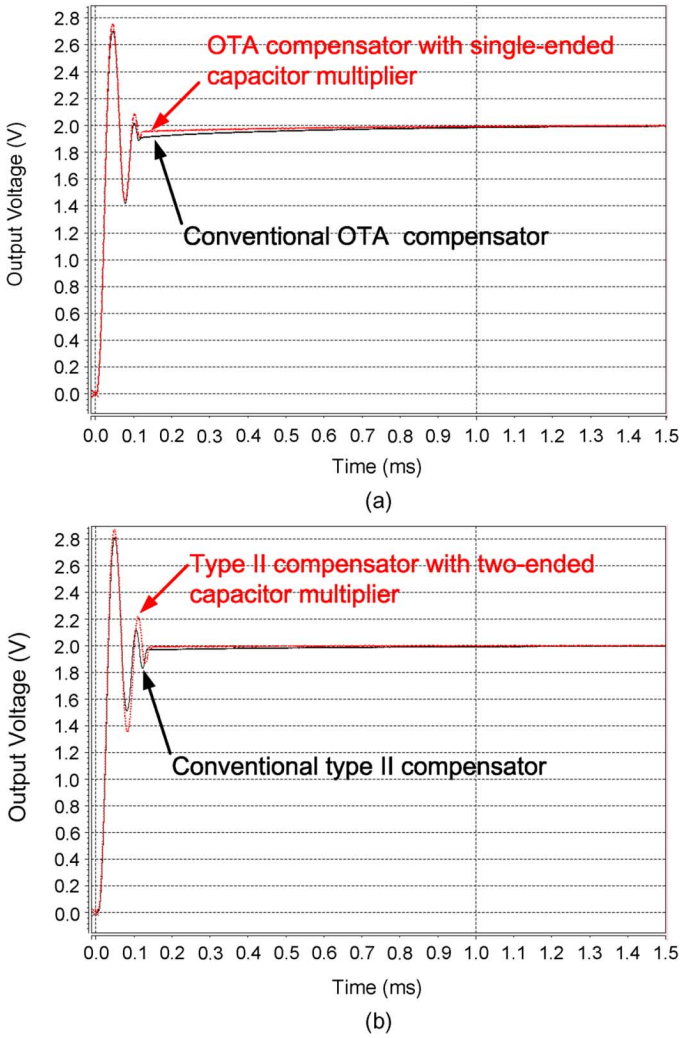

Fig. 13. Transient responses of the dc-dc buck converter when start-up without the implementation of soft-start mechanism. (a) The result compensated by OTA compensator with the single-ended capacitor multiplier and that with conventional off-chip compensation. (b) The result compensated by type II compensator with the two-ended capacitor multiplier and that with conventional off-chip compensation.

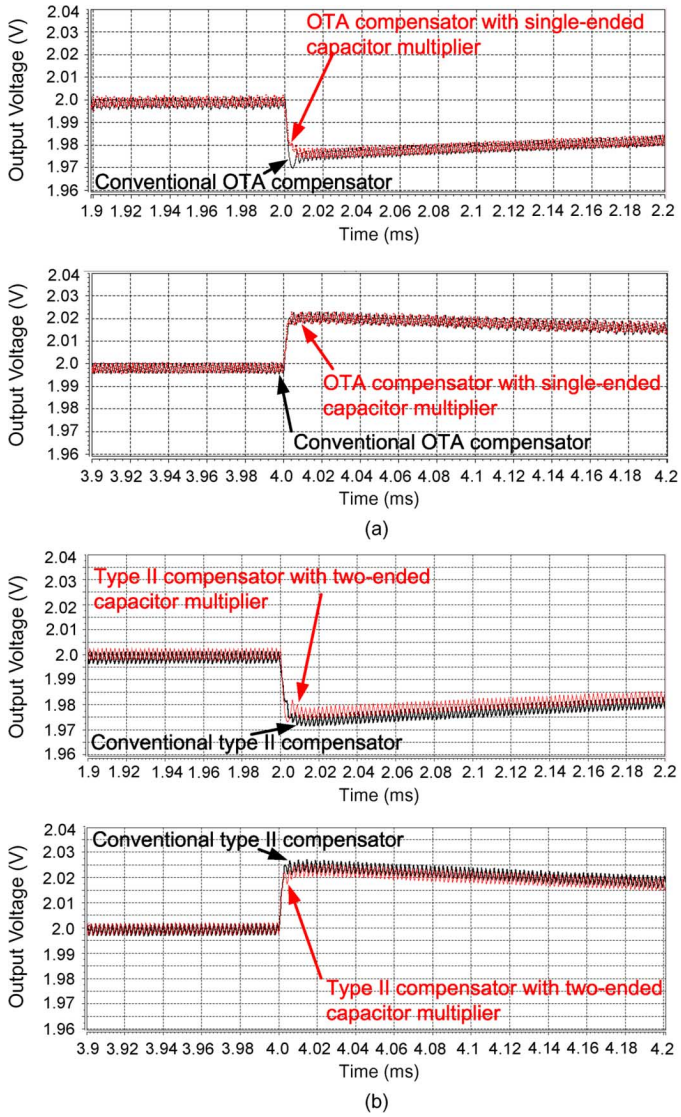

Fig. 14. Load transient responses of the dc-dc buck converter when load current stepped from 10 mA to 400 mA and 400 mA to 10 mA. (a) The result compensated by OTA compensator with the single-ended capacitor multiplier and that with conventional off-chip compensation. (b) The result compensated by type II compensator with the two-ended capacitor multiplier and that with conventional off-chip compensation.

The voltage follower implementation is shown in Fig. 6(c) [15]

$$T(s) = -\frac{1}{s(C_1+C_2)R_1} \cdot \frac{1+sC_1R_2}{1+\frac{sC_1C_2R_2}{C_1+C_2}} \tag{8}$$

and in (9) where p_1 and g_{m0} are the dominant pole and dc transconductance at the first stage of the voltage follower, respectively. C_{c1} and R_{c1} are the components of Miller compensation. The output impedance of first stage and second stage of voltage follower are r_{o1} and r_{o2}, and g_{m7} is the transconductance of the second stage. Two equivalent resistances of NMOS transistors are also modeled as R and KR. A simple representation could be obtained as

$$T(s) \approx -\frac{1}{sKC_{z1}R_1} \frac{1+sC_{z1}KR_2}{1+sC_2R_2}. \tag{10}$$

Most importantly, the value of $C_{c1}r_{o1}$ should be much smaller than those values of $C_{z1}KR_2$ and C_2R_2. Then, (10) is similar to (8) since the value of capacitor C_1 is much larger than that of C_2. According to (10), the small capacitor C_{z1} is effectively multiplied by a factor of K. Therefore, a large-valued capacitor is also built by proposed two-ended bidirectional capacitor multiplier technique.

B. Verification of the Compensation Achieved by the Two-Ended Capacitor Multiplier in Type II Compensator

Fig. 13 shows the simulation results of the dc-dc converter with OTA compensator and type II compensator when start-up. The transient simulation result of the dc-dc converter of the proposed single-ended or two-ended capacitor multiplier architecture is the same as that of the conventional design with off-chip compensation.

The load current are stepped from 10 to 400 mA and back to 10 mA with rising and falling time of 2 μs. Fig. 14 shows the

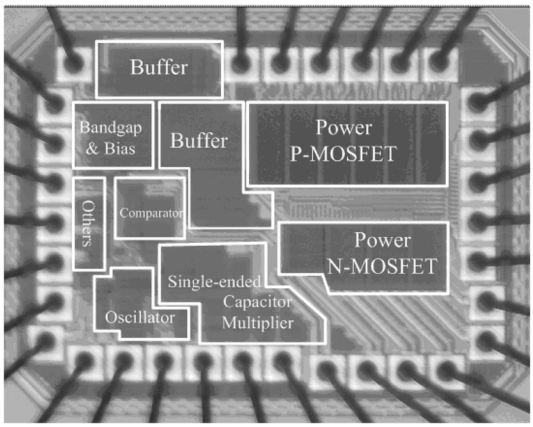

Fig. 15. Micrograph of the chip.

TABLE I
SPECIFICATIONS OF THE CURRENT-MODE DC-DC BUCK CONVERTER WITH BIDIRECTIONAL CURRENT MODE CAPACITOR MULTIPLIER TECHNIQUE

Specification	Value
Technology	TSMC 2P4M 0.35um
Input voltage	2.7V~4.5V
Output voltage	1.8V
Switching frequency	1MHz
Output current range	100mA~500mA
Inductor	8uH
Capacitor	8uF
Normal multiplied factor (K)	41
Soft-start multiplied factor (K)	441

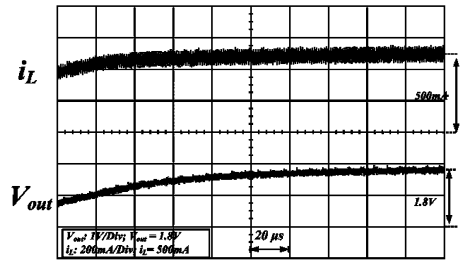

Fig. 16. Output waveform with the implementation of soft-start mechanism.

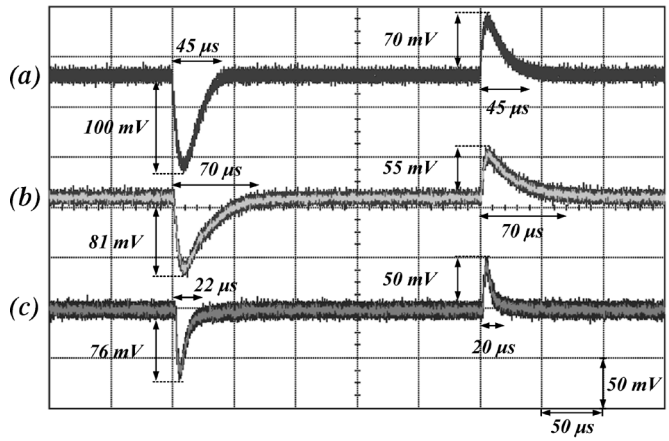

Fig. 17. Output transient waveforms of dc-dc converters with load current stepping between 100 and 500 mA. (a) Conventional design with off-chip compensation. (b) With adaptive frequency control technique [17]. (c) With the fast transient provided by the single-ended capacitor multiplier.

load transient responses in case of load current variations. Obviously, there is not any oscillation phenomenon in the simulation results. It means that the stability of current mode controlled dc-dc buck converter with proposed single-ended or two-ended capacitor multiplier architecture is the same as that of the conventional design with off-chip compensation.

IV. VERIFICATION AND EXPERIMENTAL RESULTS

The results of the proposed single-ended bidirectional current mode capacitor multiplier dc-dc converter are demonstrated by TSMC double-poly quadruple-metal 0.35-μm CMOS technology. The threshold voltages of nMOSFET and pMOSFET are 0.55 and 0.65 V, respectively. The chip micrograph is shown in Fig. 15, and the active silicon area is $1315\ \mu\text{m} * 1430\ \mu\text{m}$, including the testing pads.

The specification of current-mode dc-dc buck converter and the system compensator with single-ended bidirectional current mode capacitor multiplier technique is listed in Table I. The current flowing through a small capacitor is effectively amplified by the factor of 41 for normal compensation or 441 for soft-start mechanism. Table II lists the parasitic parameters used by the buck dc-dc converter with and without single-ended bidirectional current mode capacitor multiplier technique.

The start-up waveforms with proposed soft-start method are shown in Fig. 16. The output voltage is smoothly increasing without the overshoot issue. Besides, the inductor is also increased by a controlled rate to alleviate the inrush inductor current occurring in the start-up period. To estimate the load transient response, the load current is stepped from 100 mA to 500 mA and back to 100 mA. Fig. 17 shows the transient responses for load-current rising and falling variations. The stability is promised by our proposed technique in case of load variations. Furthermore, the transient speed by our proposed technique is faster than conventional control by about 2 times, and there is only about 76% dropout voltage of the conventional design with off-chip compensation. Obviously, there is an oscillating problem existed in our proposed method compared to the technique proposed by [17]. Thus, the control of fast transient is needed to be guaranteed under any worst conditions. In other words, it is important to make a tradeoff between the stability and the performance of low-dropout voltage.

V. CONCLUSION

A dc-dc converter with the bidirectional current mode capacitor multiplier technique that provides on-chip compensation, soft-start, and fast transient mechanisms is proposed in this paper. The bidirectional current mode capacitor multiplier technique can effectively modify the position of the crossover frequency to a suitable position for improving the response time in case of load variations and smoothing the rising of the output voltage in case of start-up period. Experimental results demonstrate the transient speed by our proposed technique is faster than that by conventional control about two times, and there is about 76% dropout voltage of the conventional design. Both the number of components on printed circuit board and the pins of

TABLE II
EXPERIMENTAL RESULTS OF THE BUCK DC–DC CONVERTER WITH AND WITHOUT SINGLE-ENDED BIDIRECTIONAL CURRENT MODE CAPACITOR MULTIPLIER TECHNIQUE

Parameter	With single-endedbidirectional current mode capacitor multiplier technique	With external compensation resistors and capacitors
R_c	165k	165k
C_{c1}	3.53p	145p
DC gain of the OTA	72dB	72dB
Compensation Zero	6.6kHz	6.6kHz
Compensation Pole	15.7Hz	15Hz

the IC package are reduced at the sacrifice of more quiescent current about $10 \sim 20\,\mu$A. With the proposed bidirectional current mode capacitor multiplier technique, the performance of dc-dc converters is improved significantly and the external pins and footprint area are minimized.

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